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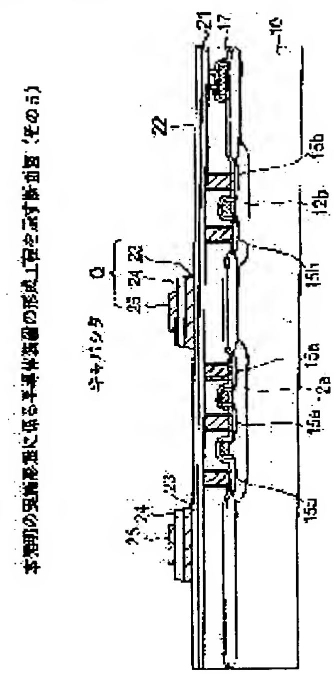
(54) MAGNETIC MEMORY DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To suppress deterioration of characteristics of a ferroelectric capacitor as to a semiconductor device which has the ferroelectric capacitor.
SOLUTION: The semiconductor device includes an insulating film 22 formed on a semiconductor substrate 10, a 1st electrode 23 of the capacitor formed on the insulating film 22, a ferroelectric film 24 which is formed on the 1st electrode 23 by an MOCVD method and of ≤1 × 1019 pieces/cm3 in the density of particles having reducing operation, and a 2nd electrode 25 of the capacitor Q formed on the ferroelectric film 24.



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CLAIMS

[Claim(s)]
[Claim 1] The concentration of the particle which is formed of CVD on the insulator layer formed on the semi-conductor substrate, the 1st electrode of the capacitor formed on said insulator layer, and said 1st electrode, and has a reduction operation is 3 1x1019 pieces/cm. Semiconductor device characterized by having the ferroelectric film for said capacitors which is the following, and the 2nd electrode of said capacitor formed on said ferroelectric film.
[Claim 2] Said particle is a semiconductor device according to claim 1 characterized by being a hydrogen atom or a heavy hydrogen atom at least.
[Claim 3] Said ferroelectric is a semiconductor device according to claim 1 or 2 characterized by being a PZT system ingredient or Bi layer structure compound ingredient.
[Claim 4] The process which forms the 1st electrode of a capacitor through an insulator layer on a semi-conductor substrate, The process which forms the ferroelectric film of said capacitor with a CVD method on said 1st electrode, In the manufacture approach of a semiconductor device of having the process which forms the 2nd electrode of said capacitor on said ferroelectric film, and the process which forms the film above said capacitor, at the process after forming said ferroelectric film It is the concentration of a particle with a reduction operation into said ferroelectric film 1x1019 pieces/cm 3 The manufacture approach of the semiconductor device characterized by making it the following.
[Claim 5] The process which forms a transistor in a semi-conductor substrate, and the process which forms the 1st electrode of a capacitor through an insulator layer on said semi-conductor substrate, In the manufacture approach of a semiconductor device of having the process which forms the ferroelectric film of said capacitor on said 1st electrode, the process which forms the 2nd electrode of said capacitor on said ferroelectric film, and the process which forms the film above said capacitor The concentration of the particle which has the reduction operation in said ferroelectric film at the process after forming said capacitor is 3 1x1019 pieces/cm. On the conditions which become the following The manufacture approach of the semiconductor device characterized by having the process which heats said semi-conductor substrate in a hydrogen content ambient atmosphere in order to improve the property of said transistor.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device which has a ferroelectric capacitor in more detail about a semiconductor device.
[0002]
[Description of the Prior Art] Even if it turns off the power, information can be held, and ferroelectric nonvolatile memory (FeRAM) attracts attention as memory which can moreover perform writing and read-out in power saving. FeRAM has the memory cell which consists of a transfer transistor and a ferroelectric capacitor. The ferroelectric capacitor has the structure which sandwiched the ferroelectric film with the lower electrode and the up electrode.
[0003] the ferroelectric film which constitutes a ferroelectric capacitor -- Bi layer structure compound ingredients, such as PZT system ingredients, such as titanic-acid lead zirconate (PZT) and the La dope PZT (PLZT), and SrBi2Ta 2O9 (SBT, Y1), SrBi2(Ta, Nb)2O9 (SBTN, YZ), etc. -- it is -- those ingredients -- a sol gel process, a spatter, and MOCVD -- membranes are formed by law etc.
[0004] Usually, the ferroelectric film crystallizes the ferroelectric film to a perovskite structure by heat treatment, after forming the ferroelectric film of an amorphous phase on a lower electrode. Subsequently, an up electrode is formed on the ferroelectric film and capacitor structure is acquired.
[0005] It is common to use platinum (Pt) as an ingredient of an up electrode. Although the up electrode using platinum has small leakage current and there is an advantage, like the hysteresis curve of the polarization property of a capacitor can be enlarged, it is known that a fatigue property is bad, that degradation in the process in which a semiconductor device is made is large, and that dependability is bad. About such a Pt up electrode, it will be Japan Society of Applied Physics 29 a-K -4 for example, in autumn (59 times) of 1998. There is a publication.
[0006] In order to solve the trouble of Pt up electrode, development of the up electrode which used oxidation electric conduction material, such as IrO2 and SrRuO3 (SRO), is performed. About forming an up electrode from IrO2, ISIF 2000 and 12 th International Symposium on IntergratedFerroelectrics Nop.017C have a publication, for example. Moreover, about using the up electrode which consists of SRO, Japan Society of Applied Physics 2 p-A -6 will have a publication in spring (60 times) of 1999, for example.
[0007] By using the electrode which consists of a conductive oxide ingredient like them IrO2 and SRO, a fatigue property and degradation can be controlled and dependability can be improved.
[0008] On the other hand, it is known well that reducing atmosphere, especially a hydrogen atom will degrade the property of a ferroelectric. Therefore, the approach of forming a semiconductor device, as a ferroelectric and hydrogen are not contacted has been taken. K.Kushida-A., J.Appl.Phys, .85, 1069, and 1999 **** -- PbO formed on the up electrode Preventing the diffusion to the ferroelectric film of the hydrogen which penetrates an up electrode with the film is reported. [for example,]
[0009] moreover, TiO which does not let water pass between a ferroelectric and an interlayer film in the patent No. 3157734 official report etc. -- the film was formed and diffusion of the

hydrogen to a ferroelectric is prevented.
[0010] Furthermore, at JP,8-37282,A, it is the hydrogen atom concentration in an interlayer film 10x1021 pieces/cm 3 It is shown that degradation of the ferroelectric film resulting from a hydrogen atom can be controlled by making it below.
[0011]
[Problem(s) to be Solved by the Invention] It may be able to stop however, being able to aim at an improvement of component properties other than a capacitor by the various structures conventionally adopted in order to prevent reduction of a ferroelectric capacitor being what increases the process of semiconductor device manufacture, or avoiding a hydrogen process superfluously.
[0012] The purpose of this invention is to offer the semiconductor device which can control degradation of a ferroelectric capacitor property, and its manufacture approach.
[0013]
[Means for Solving the Problem] The insulator layer by which the above-mentioned technical problem was formed on the semi-conductor substrate, and the 1st electrode of the capacitor formed on said insulator layer, The concentration of the particle which is formed of CVD on said 1st electrode, and has a reduction operation is 3 1x1019 pieces/cm. Ferroelectric film for said capacitors which is the following, It is solved by the semiconductor device characterized by having the 2nd electrode of said capacitor formed on said ferroelectric film.
[0014] Moreover, the process at which the above-mentioned technical problem forms the 1st electrode of a capacitor through an insulator layer on a semi-conductor substrate, The process which forms the ferroelectric film of said capacitor with a CVD method on said 1st electrode, In the manufacture approach of a semiconductor device of having the process which forms the 2nd electrode of said capacitor on said ferroelectric film, and the process which forms the film above said capacitor, at the process after forming said ferroelectric film It is the concentration of a particle with the reduction operation in said ferroelectric film 1x1019 pieces/cm 3 It is solved by the manufacture approach of the semiconductor device characterized by making it the following.
[0015] Moreover, the process at which the above-mentioned technical problem forms a transistor in a semi-conductor substrate, The process which forms the 1st electrode of a capacitor through an insulator layer on said semi-conductor substrate, In the manufacture approach of a semiconductor device of having the process which forms the ferroelectric film of said capacitor on said 1st electrode, the process which forms the 2nd electrode of said capacitor on said ferroelectric film, and the process which forms the film above said capacitor On the conditions from which the concentration of a particle with the reduction operation in said ferroelectric film becomes less than [1x1019 //cm] three at the process after forming said capacitor In order to improve the property of said transistor, it is solved by the manufacture approach of the semiconductor device characterized by having the process which heats said semi-conductor substrate in a hydrogen content ambient atmosphere.
[0016] It is total of the concentration of the particle which has the reduction operation in the ferroelectric film according to this invention, for example, the concentration of a hydrogen atom and a heavy hydrogen atom, 1x1019 pieces/cm 3 Since it considered as the following, degradation of the ferroelectric resulting from hydrogen, heavy hydrogen, etc. was prevented, the property of a ferroelectric capacitor could be controlled, and things became clear by experiment.
[0017] Moreover, it is total of a hydrogen atom and a heavy hydrogen atom 1x1017 pieces/cm 3 By considering as the following, degradation of a capacitor property can be prevented further.
[0018]
[Embodiment of the Invention] The operation gestalt of this invention is explained based on a drawing below.
[0019] Drawing 1 - drawing 16 are the sectional views showing the manufacture approach of the semiconductor device of 1 operation gestalt of this invention in order of a process. In addition, as a semiconductor device of this operation gestalt, FeRAM is mentioned as an example and explained.
[0020] First, a process until it acquires the cross-section structure shown in drawing 1 is explained.

[0021] it is shown in drawing 1 -- as -- p-type silicon (semi-conductor) substrate 10 front face -- LOCOS (Local Oxidation of Silicon) -- the isolation insulator layer 11 is alternatively formed by law. STI (Shallow Trench Isolation) may be adopted as an isolation insulator layer 11.
[0022] Then, p mold impurity and n mold impurity are alternatively introduced into the predetermined active region (transistor formation field) in the memory cell field 1 of a silicon substrate 10, and the circumference circuit field 2, and p well 12a and n well 12b are formed. In addition, in the circumference circuit field 2, although not shown in drawing 1 , in order to form CMOS, p well (un-illustrating) is also formed.
[0023] Then, the active-region front face of a silicon substrate 10 is oxidized thermally, and silicon oxide is formed as gate-dielectric-film 10a.
[0024] Next, sequential formation of the amorphous silicon film and the tungsten silicide film is carried out all over a silicon substrate 10 top, patterning of these amorphous silicon film and the tungsten silicide film is carried out to a predetermined configuration by the photolithography method, and the gate electrodes 13a-13c and wiring 14 are formed. In addition, the polish recon film may be formed instead of the amorphous silicon film which constitutes the gate electrodes 13a-13c.
[0025] On [of one] p well 12a, two gate electrodes 13a and 13b are arranged at juxtaposition, and those gate electrodes 13a and 13b constitute a part of word line WL from a memory cell field 1.
[0026] Next, in the memory cell field 1, in p well 12a of the both sides of the gate electrodes 13a and 13b, the ion implantation of the n mold impurity is carried out, and n mold impurity diffusion field 15a used as the source drain of an n channel MOS transistor is formed. It can come, simultaneously n mold impurity diffusion field may be formed also in p well (un-illustrating) of the circumference circuit field 2.

TECHNICAL FIELD

[Field of the Invention] This invention relates to the semiconductor device which has a ferroelectric capacitor in more detail about a semiconductor device.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Even if it turns off the power, information can be held, and ferroelectric nonvolatile memory (FeRAM) attracts attention as memory which can moreover perform writing and read-out in power saving. FeRAM has the memory cell which consists of a transfer transistor and a ferroelectric capacitor. The ferroelectric capacitor has the structure which sandwiched the ferroelectric film with the lower electrode and the up electrode.
[0003] the ferroelectric film which constitutes a ferroelectric capacitor -- Bi layer structure compound ingredients, such as PZT system ingredients, such as titanic-acid lead zirconate (PZT) and the La dope PZT (PLZT), and SrBi2Ta 2O9 (SBT, Y1), SrBi2(Ta, Nb)2O9 (SBTN, YZ), etc. -- it is -- those ingredients -- a sol gel process, a spatter, and MOCVD -- membranes are formed by law etc.
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[0005] It is common to use platinum (Pt) as an ingredient of an up electrode. Although the up electrode using platinum has small leakage current and there is an advantage, like the hysteresis curve of the polarization property of a capacitor can be enlarged, it is known that a fatigue property is bad, that degradation in the process in which a semiconductor device is made is large, and that dependability is bad. About such a Pt up electrode, it will be Japan Society of Applied Physics 29 a-K -4 for example, in autumn (59 times) of 1998. There is a publication.
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EFFECT OF THE INVENTION

[Effect of the Invention] According to [as stated above] this invention, it is total of the concentration of the hydrogen atom of the ferroelectric film, and a heavy hydrogen atom 1x1019 pieces/cm 3 Since it considered as the following, degradation of the ferroelectric resulting from hydrogen or heavy hydrogen was prevented, the property of a ferroelectric capacitor could be controlled, and things became clear by experiment. Moreover, it is total of a hydrogen atom and a heavy hydrogen atom 1x1017 pieces/cm 3 By considering as the following, the effectiveness can be heightened further.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] It may be able to stop however, being able to aim at an improvement of component properties other than a capacitor by the various structures conventionally adopted in order to prevent reduction of a ferroelectric capacitor being what increases the process of semiconductor device manufacture, or avoiding a hydrogen process superfluously.
[0012] The purpose of this invention is to offer the semiconductor device which can control degradation of a ferroelectric capacitor property, and its manufacture approach.

[Translation done.]

MEANS

[Means for Solving the Problem] The insulator layer by which the above-mentioned technical problem was formed on the semi-conductor substrate, and the 1st electrode of the capacitor formed on said insulator layer, The concentration of the particle which is formed of CVD on said 1st electrode, and has a reduction operation is 3 1x1019 pieces/cm. Ferroelectric film for said capacitors which is the following, It is solved by the semiconductor device characterized by having the 2nd electrode of said capacitor formed on said ferroelectric film.
[0014] Moreover, the process at which the above-mentioned technical problem forms the 1st electrode of a capacitor through an insulator layer on a semi-conductor substrate, The process which forms the ferroelectric film of said capacitor with a CVD method on said 1st electrode, In the manufacture approach of a semiconductor device of having the process which forms the 2nd electrode of said capacitor on said ferroelectric film, and the process which forms the film above said capacitor, at the process after forming said ferroelectric film It is the concentration of a particle with the reduction operation in said ferroelectric film 1x1019 pieces/cm 3 It is solved by the manufacture approach of the semiconductor device characterized by making it the following.
[0015] Moreover, the process at which the above-mentioned technical problem forms a transistor in a semi-conductor substrate, The process which forms the 1st electrode of a capacitor through an insulator layer on said semi-conductor substrate, In the manufacture approach of a semiconductor device of having the process which forms the ferroelectric film of said capacitor on said 1st electrode, the process which forms the 2nd electrode of said capacitor on said ferroelectric film, and the process which forms the film above said capacitor On the conditions from which the concentration of a particle with the reduction operation in said ferroelectric film becomes less than [1x1019 //cm] three at the process after forming said capacitor In order to improve the property of said transistor, it is solved by the manufacture approach of the semiconductor device characterized by having the process which heats said semi-conductor substrate in a hydrogen content ambient atmosphere.
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[0023] Then, the active-region front face of a silicon substrate 10 is oxidized thermally, and silicon oxide is formed as gate-dielectric-film 10a.
[0024] Next, sequential formation of the amorphous silicon film and the tungsten silicide film is carried out all over a silicon substrate 10 top, patterning of these amorphous silicon film and the tungsten silicide film is carried out to a predetermined configuration by the photolithography method, and the gate electrodes 13a-13c and wiring 14 are formed. In addition, the polish recon film may be formed instead of the amorphous silicon film which constitutes the gate electrodes 13a-13c.
[0025] On [of one] p well 12a, two gate electrodes 13a and 13b are arranged at juxtaposition, and those gate electrodes 13a and 13b constitute a part of word line WL from a memory cell field 1.
[0026] Next, in the memory cell field 1, in p well 12a of the both sides of the gate electrodes 13a and 13b, the ion implantation of the n mold impurity is carried out, and n mold impurity diffusion field 15a used as the source drain of an n channel MOS transistor is formed. It can come, simultaneously n mold impurity diffusion field may be formed also in p well (un-illustrating) of the circumference circuit field 2. Then, in the circumference circuit field 2, the ion implantation of the p mold impurity is carried out to n well 12b of the both sides of gate electrode 13c, and p mold impurity diffusion field 15b used as the source drain of a p channel MOS transistor is formed. n mold impurity and p mold impurity -- having good control of striking a ball in any direction -- it is carried out using a resist pattern.
[0027] After that, after forming an insulator layer all over a silicon substrate 10, etchback of the insulator layer is carried out, and it leaves the gate electrodes 13a-13c and the both-sides part of wiring 14 as a side-attachment-wall insulator layer 16. as the insulator layer -- for example, CVD (chemical vapor deposition) -- silicon oxide (SiO_2) is formed by law.
[0028] Furthermore, n mold impurity diffusion field 15a is made into LDD structure by using the gate electrodes 13a and 13b and the side-attachment-wall insulator layer 16 for a mask, and carrying out the ion implantation of the n mold impurity again into n mold impurity diffusion field 15a of the memory cell field 1. n mold impurity diffusion field 15a in the circumference circuit field 2 is also made into LDD structure at this and coincidence. Moreover, p mold impurity diffusion field is made into LDD structure by carrying out the ion implantation of the p mold impurity again into p mold impurity diffusion field 15b in the circumference circuit field 2.
[0029] Two MOS transistors T1 which have n mold impurity diffused layer 15a of the gate electrodes 13a and 13b and LDD structure in p well 12a according to the above process, and T2 It is formed. Moreover, MOS transistor T3 which has gate electrode 13c and p mold impurity diffused layer 15b of LDD structure in n well 12b It is formed.
[0030] Next, the acid silicon nitride (SiON) film with a thickness of about 200nm is formed for an MOS transistor all over a silicon substrate 10 by the plasma-CVD method as wrap covering film. Then, silicon oxide (SiO_2) of about 1.0 micrometers of thickness is grown up on the covering film 3 as the 1st interlayer insulation film 17 by the plasma-CVD method using TEOS gas.
[0031] Then, the 1st interlayer insulation film 17 is heat-treated for 30 minutes at the temperature of 700 degrees C in the nitrogen-gas-atmosphere mind of ordinary pressure as eburnation processing of the 1st interlayer insulation film 17. after that -- the top face of the 1st interlayer insulation film 17 -- chemical mechanical polishing (CMP) -- flattening is carried out by law.
[0032] Next, a process until it forms the structure shown in drawing 2 is explained.
[0033] First, patterning of the covering film 3 and the 1st interlayer insulation film 17 is carried

out by the photolithography method, and beer hall 17e of the contact holes 17a-17d of the depth which arrives at the impurity diffusion fields 15a and 15b, and the depth which reaches wiring 14 is formed in the 1st interlayer insulation film 17, respectively. Then, it is TiN of Ti (titanium) thin film of 20nm of thickness, and 50nm of thickness to the 1st interlayer insulation film 17 top face and hole 17a - 17e inside. A thin film (titanium night RAIDO) is formed in order by the spatter. Furthermore, it is TiN about a tungsten (W) by the CVD method. It grows up on a thin film. This will be in the condition that the tungsten film was embedded in contact holes 17a-17d and beer hall 17e.

[0034] Then, the tungsten film, a TiN thin film, and Ti thin film are ground by the CMP method until the 1st interlayer insulation film 17 top face is exposed. The titanium film, titanium nitride film, and tungsten film which were left behind in hole 17a - 17e by this are used as conductive plugs 18a-18e, respectively.

[0035] 1st conductive plug 18a on n mold impurity diffusion field 15a inserted into two gate electrodes 13a and 13b in one p well 12a of the memory cell field 1 is connected to the bit line mentioned later, and conductive plug 18of ** remaining two 2nd b is further connected to the capacitor mentioned later.

[0036] Next, as shown in drawing 3 , the SiON (insulator layer) film 21 is formed on the conductive plugs 18a-18e the 1st interlayer insulation film 17 top by the plasma-CVD method using a silane and ammonia at the thickness of 120nm. This SiON film 21 is formed in order to prevent oxidation of the conductive plugs 18a-18e. Furthermore, SiO2 film 22 with a thickness of 150nm is formed on the SiON film 21 by the plasma-CVD method using TEOS and oxygen as reactant gas. In addition, SiO2 film 22 is formed in order to prevent invasion of the water to the 1st interlayer insulation film 17.

[0037] Then, those film is heat-treated for 30 minutes at the temperature of 650 degrees C in the nitrogen-gas-atmosphere mind of ordinary pressure for the eburnation of the SiON film 21 and SiO2 film 22.

[0038] Next, as shown in drawing 4 , by DC spatter, platinum of titanium of 10-30nm of thickness and 100-300nm of thickness is formed pure on SiO2 film 22, and the 1st electric conduction film of the two-layer structure is formed. In addition, film, such as iridium, a ruthenium, ruthenium oxide, oxidization iridium, and ruthenium oxide strontium (SrRuO3), may be formed as 1st electric conduction film 23a.

[0039] Then, the lanthanum calcium strontium doped titanic-acid lead zirconate (PLCSZT) film is formed by the spatter as ferroelectric film 24a on 1st electric conduction film 23a with RF spatter at the thickness of 100-300nm, for example, 200nm.

[0040] Spatter conditions are 1.0Pa and RF power 1kW using Ar gas using PLCSZT sintered as a target. There is no process which puts the PLCSZT film into hydrogen or heavy hydrogen during this processing, and mixing of the hydrogen to the inside of the PLCSZT film and heavy hydrogen cannot be considered. Moreover, the concentration of the hydrogen in the PLCSZT film after annealing and heavy hydrogen is 3 1x1019 pieces/cm so that it may mention later. as-depo of the PLCSZT film since it is the following The concentration of the hydrogen in the film or heavy hydrogen is also 3 1x1019 pieces/cm. That it is the following can presume easily. In addition, it is also the same as when forming the PZT system ingredient film instead of the PLCSZT film.

[0041] Then, it is RTA (Rapid Thermal Annealing) in an oxygen ambient atmosphere as crystallization processing of ferroelectric film 24a at the temperature of 600-850 degrees C, and the conditions for 30 - 120 seconds. It carries out. For example, it anneals for 60 seconds at the temperature of 750 degrees C.

[0042] everything but the spatter described above as the formation approach of the ferroelectric ingredient film -- the spin turning-on method, a sol-gel method, and MOD (Metal Organi Deposition) law and MOCVD (organic metal CVD) -- law -- it is -- MOCVD -- about law, it mentions later.

[0043] As an ingredient of ferroelectric film 24a, you may be other PZT system ingredients like PZT and PLZT, SrBi2Ta 2O9 and Bi layer structure compound ingredient of SrBi2(Ta, Nb)2O9 grade, and other metallic-oxide ferroelectrics besides PLCSZT.

[0044] After forming such ferroelectric film 24a, the oxidization iridium (IrO2) film is formed by

the spatter as 2nd electric conduction film 25a on it at the thickness of 100-300nm. In addition, Pt film or the SRO film may be formed by the spatter as 2nd electric conduction film 25a.
[0045] Next, a resist is applied on 2nd electric conduction film 25a, a resist is exposed and developed further, and patterning is carried out to an up electrode configuration. After that, dry etching of the 2nd electric conduction film 25a is carried out to a mask using a resist pattern, and 2nd electric conduction film 25a is used as the up electrode 25 of a capacitor. Ashing of the resist is carried out by the oxygen plasma, and it is removed next.
[0046] Next, ferroelectric film 24a which received the damage by the pattern formation of the up electrode 25 is annealed on 650 degrees C and the conditions for 60 minutes in an oxygen ambient atmosphere, and this improves the membraneous quality of the ferroelectric film. The concentration of particles, such as a particle with the reduction operation in ferroelectric film 24a by this, for example, hydrogen, and heavy hydrogen, is 3 1x1017 pieces/cm. It is the following.
[0047] To next, it is aluminum 2O3. Although the becoming protective coat may be formed on the up electrode 25 and ferroelectric film 24a, it omits, in forming ferroelectric film 24a by the spatter.
[0048] Then, patterning of ferroelectric 24a and the 1st electric conduction film 23a is carried out one by one by the photolithography method. In addition, after carrying out patterning of the 1st electric conduction film 23a, it heats for 60 minutes at the temperature of 650 degrees C within an oxygen content ambient atmosphere, and the membraneous quality of ferroelectric film 24a is improved.
[0049] Thereby, ferroelectric film 24a becomes the dielectric film 24 for capacitors, and 1st electric conduction film 23a becomes the lower electrode 23 for capacitors. And Capacitor Q is constituted by the up electrode 25, a dielectric film 24, and the lower electrode 23.
[0050] After forming Capacitor Q through the above processes, as it is shown in drawing 6 , the 2nd interlayer insulation film 26 of the two-layer structure which consists of SiO2 film and SOG film is formed in the whole surface, and it is a wrap about Capacitor Q by this 2nd interlayer insulation film 26. The SiO2 film is formed by the thickness of 100-300nm all over a silicon substrate 10 top of the plasma-CVD method for using TEOS gas by the conditions whose growth temperature is 390 degrees C and whose power is 400W. Moreover, the SOG film is formed by heating this, after applying an SOG solution to the thickness of 80-200nm on the TEOS film.
[0051] And patterning of the 2nd interlayer insulation film 26 is carried out by the photolithography method, and contact hole 26a is formed on the up electrode 25 of Capacitor Q. Then, recovery annealing is carried out to a dielectric film 24. Specifically, it heats for 30 - 120 minutes at the temperature of 500-650 degrees C in an oxygen ambient atmosphere.
[0052] Next, patterning of the 2nd interlayer insulation film 26, the SiON film 21, and the SiO2 film 22 is carried out by the photolithography method, contact hole 26b is formed on 2nd conductive plug 18b of the memory cell field 1, and 2nd conductive plug 18b is exposed. And it is TiN of 100nm of thickness the 2nd interlayer insulation film 26 top and in contact hole 26a and 26b. The film is formed by the spatter. Then, the TiN By carrying out patterning of the film by the photolithography method, the partial wiring (local wiring) 27 for carrying out electrical installation of 2nd conductive plug 18b on p well 12a and the capacitor up electrode 25 through contact holes 26a and 26b in the memory cell field 1 is formed.
[0053] Next, a process until it forms structure as shown in drawing 7 is explained.
[0054] First, the TEOS film is formed by the plasma-CVD method on the partial wiring 27 and the 2nd interlayer insulation film 26 at the thickness of 200-400nm. This TEOS film is used as the 3rd interlayer insulation film 31.
[0055] Then, while forming contact hole 31a on 1st conductive plug 18a of the mid gear of p well 12a by carrying out patterning of from the 3rd interlayer insulation film 31 in the memory cell field 1 to the SiON film 21 of the lower part by the photolithography method, contact holes 31c-31e are formed also on each conductive plug 18c-18e of the circumference circuit field 2.
[0056] Furthermore, they are Ti film and TiN in the 3rd interlayer insulation film 31 top and contact holes 31c-31e. The film, aluminum (aluminum) film, and TiN While forming bit line 32a in the memory cell field 1 by carrying out the laminating of the four layers of the film one by one,

and carrying out patterning of these metal membranes, in the circumference circuit field 2, Wiring 32c-32e is formed. These bit line 32a and Wiring 32c-32e turn into aluminum wiring of an eye further.

[0057] In addition, bit line 32a of the memory cell field 1 is connected to 1st conductive plug 18a, and the wiring 32c-32e of the circumference circuit field 2 is connected to each conductive plugs 18c-18e.

[0058] It is TiN of the thickness of 20nm, and the bottom about Ti film of for example, the lowest layer as thickness of each metal membrane which constitutes bit line 32a and Wiring 32c-32e. It is TiN of the thickness of 500nm, and a top about the thickness of 50nm, and aluminum film in the film. Let the film be the thickness of 100nm.

[0059] Next, a process until it forms structure as shown in drawing 8 is explained.

[0060] First, the 4th interlayer insulation film 33 which consists of SiO2 [with a thickness of 2.0 micrometers] is formed after the 3rd interlayer insulation film 31, bit line 32a, and Wiring 32c-32e by the plasma-CVD method which uses TEOS gas and oxygen (O2) gas.

[0061] Furthermore, the top face of the 4th interlayer insulation film 33 is ground by the CMP method, and carries out flattening. Let the amount of polishes be thickness equivalent extent of about 1.0 micrometers from the maximum top face.

[0062] Furthermore, patterning of the 4th interlayer insulation film 33 is carried out by the photolithography method, and beer hall 33a which reaches further 32d of aluminum wiring of an eye, for example, wiring of the circumference circuit field 2, is formed.

[0063] Then, sequential formation of Ti film of 20nm of thickness and the TiN film of 50nm of thickness is carried out by sputtering, and those film is set to GRU layer 35a on the inside of beer hall 33a, and the top face of the 4th interlayer insulation film 33. Then, tungsten film 35b is formed on GRU layer 35a. Thereby, it fills up with GRU layer 35a and tungsten film 35b in beer hall 33a.

[0064] Then, the CMP method or etchback removes tungsten film 35b on the 4th interlayer insulation film 33 top face, and GRU layer 35a, and it is made to remain only in beer hall 33a.

[0065] Next, a process until it forms structure as shown in drawing 9 is explained.

[0066] First, it is the 1st TiN on the 4th interlayer insulation film 33. They are 500nm and the 2nd TiN about 50nm and aluminum film in the film. Sequential formation of the film is carried out at the thickness of 50nm. Then, the 1st and 2nd TiN(s) The aluminum wiring 36 of a bilayer eye is formed by carrying out patterning of the film and the aluminum film by the photolithography method.

[0067] Then, SiO2 film is formed as 1st covering insulator layer 37 by the plasma-CVD method using TEOS at the thickness of 200nm on the aluminum wiring 36 of a bilayer eye, and the 4th interlayer insulation film 33. Furthermore, it is SiN by the plasma-CVD method on the 1st covering insulator layer 37. The 2nd becoming covering insulator layer 38 is formed in the thickness of 500nm. The wiring 36 of a bilayer eye is covered with these 1st and 2nd covering film 37 and 38.

[0068] After that, they are MOS transistors T1 and T2 and T3. In order to improve a property, the whole is heated at 400-450 degrees C in the ambient atmosphere of hydrogen nitrogen mixed gas. The hydrogen content and heating temperature in the ambient atmosphere are set as conditions from which the concentration of particles, such as the particle which has a reduction operation in ferroelectric film 24a which constitutes Capacitor Q, for example, hydrogen, and heavy hydrogen, finally becomes less than [1x1019 //cm] three. Namely, the initial state of formation of ferroelectric film 24a to 1x1019 piece/cm3 Invasion of the reduction particle to ferroelectric film 24a of the following is permitted. For example, it sets to ferroelectric film 24a which is the capacitor dielectric film 24, and is 3 1x1019 pieces/cm from an initial state. The capacitor property by the increment in the reduction particles (heavy hydrogen, hydrogen, etc.) of the following is satisfactory.

[0069] In the condition after forming Capacitor Q with the above operation gestalten It is the concentration of the particle which has a reduction operation in ferroelectric film 24a 1x1017 pieces/cm 3 MOS transistors [from / after considering as the following and forming Capacitor Q] T1 and T2, and T3 Where the heat-treatment for a property improvement is finished The

reduction operation particle concentration in ferroelectric film 24a is 3 1x1019 pieces/cm. It is 3 1x1017 pieces/cm preferably the following. The conditions of each process are adjusted so that it may become the following. Thereby, degradation of a ferroelectric capacitor is barred.
[0070] Moreover, it sets at a process until it finishes annealing in a hydrogen content ambient atmosphere for an improvement of an MOS transistor property. The concentration of the reduction operation atom in ferroelectric film 24a of Capacitor Q is 3 1x1019 pieces/cm. In becoming above as shown in drawing 10 , after [for example,] forming the pattern of the up electrode 25 -- an up electrode 25 and ferroelectric film 24a top -- aluminum 2O3 etc. -- the protective coat 37 for reduction prevention which becomes with a metal oxide film is formed, and patterning of ferroelectric film 24a and the 1st electric conduction film 23a is carried out after that. This protective coat 37 is formed in order to control reduction of ferroelectric film 24a.
[0071] Thereby, it is in the condition which finished heat-treatment in a hydrogen content ambient atmosphere, and the concentration is 3 1x1019 pieces/cm. Adjusting so that it may become the following is possible. In addition, it is the hydrogen concentration in the oxide ferroelectric film 1x1019 pieces/cm by choosing the formation conditions and annealing conditions of interlayer insulation films 17, 26, and 33 3 The following, it carries out to less than [1x1017 //cm] three preferably, and degradation of the capacitor property Q is prevented.
[0072] next, the property of Capacitor Q of having ferroelectric film 24a formed of the spatter -- the reducing atmosphere after capacitor Q formation -- ** -- it explains [like] whether it is influenced.
[0073] First, as shown in drawing 11 , after forming the lower electrode 42 which consists of the two-layer structure of titanium layer 42a and platinum layer 42b through an insulator layer 41 on the semi-conductor substrate 40, the dielectric film film 43 was formed by the spatter a little more than [PLCSZT / of 200nm of thickness] on the lower electrode. And RTA processing of the PLCSZT ferroelectric film 43 was carried out at 600-750 degrees C in the oxygen ambient atmosphere of ordinary pressure, and membraneous quality has been improved. Furthermore, the Ir2O film of 200nm of thickness was formed by the spatter on the PLCSZT ferroelectric film 43, patterning of this was carried out to the resist using etching, and thereby, two or more Ir2O up electrodes 44 were formed, and, subsequently were heated at 650 degrees C in the oxygen ambient atmosphere.
[0074] It is one capacitor Q0 by one Ir2O up electrode 44, the PLCSZT ferroelectric film 43 under it, and the lower electrode 42. It is constituted.
[0075] Such a capacitor Q0 As a sample which it has, it is the flat-surface configuration of the up electrode 44 50x50 micrometers 2 It is [the 1st sample made into magnitude, and] the flat-surface configuration 200x200 micrometers 2 The 2nd sample made into magnitude was created.
[0076] And such a ferroelectric capacitor Q0 The 1st and 2nd samples which it has were heated at the temperature of 200 degrees C in the reducing gas content ambient atmosphere of 4.5Torr (s). Reducing gas content ambient atmospheres are the heavy hydrogen and nitrogen-gas-atmosphere mind containing 3% of heavy hydrogen (D2). Heavy hydrogen is used instead of hydrogen from the ease of concentration detection here. Moreover, the multi-statement of the heating time was carried out to 0 minute, 10 minutes, 15 minutes, and 20 minutes. In addition, it is shown that heating for 0 minute does not heat.
[0077] When heavy hydrogen concentration was investigated according to the secondary ion mold mass spectrometry (SIMS) about the 1st and 2nd samples, it is a capacitor Q0. In the part, heavy hydrogen concentration distribution as shown in the depth direction from the top face of the up electrode 44 at drawing 12 existed. Moreover, capacitor Q0 In the part in which the surrounding up electrode 44 is not formed, heavy hydrogen concentration distribution as shown in the depth direction from PLCSZT ferroelectric film 43 top face at drawing 13 existed. In addition, in drawing 12 , drawing 13 , and the following drawings, "Ir2OTEL" shows the part in which the up electrode 44 was formed, and "no Ir2O TEL" shows the part where the up electrode 44 was removed by etching.
[0078] If there is no suitable means to measure the hydrogen concentration in a sample by SIMS and the experiment approach and the meaning are taken into consideration, whether replace the concentration of heavy hydrogen with hydrogen concentration, and it considers it or it replaces

with the concentration of a particle with a reduction operation, extent of reduction capacity can be known and it will be satisfactory.
[0079] When it expressed with the bar graph what kind of effect it would have on the heavy hydrogen atom concentration in the PLCSZT ferroelectric film of the 1st and 2nd samples by the difference in heat time amount and being compared based on drawing 12 and drawing 13 , it came to be shown in drawing 14 .
[0080] In drawing 14 , "TEL" shows D concentration of the part covered with the up electrode 44 among the PLCSZT ferroelectric film 43, and "NoTEL" shows D concentration of the part into which the up electrode 44 was etched among the PLCSZT ferroelectric film 43.
[0081] The PLCSZT ferroelectric film 43 Q0 which is covered with the up electrode 44 according to drawing 14 , i.e., a capacitor, D concentration in the constituted PLCSZT ferroelectric film 43 was hardly increasing with heating by the heavy hydrogen and nitrogen-gas-atmosphere mind for about 10 minutes. However, D concentration in the PLCSZT ferroelectric film 43 of the part which is not covered with the up electrode 44 is 8x1018-/cm3 by heating for about 10 minutes. It went up to extent.
[0082] Furthermore, capacitor Q0 of the 2nd sample in the condition (0 minute) of not heating Capacitor Q0 of the 2nd sample after 10 minutes, 15 minutes, and 20-minute heating When the pulse voltage of **3V was impressed to each and the electrical potential difference and the polarization property were investigated, the result as shown in drawing 15 was obtained.
[0083] with reference to the graph of "TEL" of drawing 14 , heavy hydrogen concentration (D) increases the amount (Qsw) of polarization charge shown in drawing 15 so that clearly -- it is alike, and it follows and becomes small. According to the experiment of this invention persons, heavy hydrogen concentration is 1x1019-/cm3. When it became above, it wrote in as a FeRAM cel and changed into the condition of being easy to produce an error in read-out. Here, heavy hydrogen (D) concentration is equivalent to hydrogen (H) concentration, and reduction atom concentration is 1x1019-/cm3. Becoming the following is desirable.
[0084] Next, about the 1st sample of 1cmx1cm magnitude, when measured with the temperature-programmed-desorption analysis method (TDS), respectively, the result as shown in drawing 16 and drawing 17 was obtained [thing / the thing in the condition of not heating, and / which was heated for 20 minutes in the heavy hydrogen content ambient atmosphere]. Measurement of TDS was performed by carrying out the temperature up of the 1st sample from ordinary temperature to 750 degrees C with the programming rate of 1 degree C/second while placing the 1st sample into the vacuum ambient atmosphere.
[0085] The 1st sample heated for 20 minutes in the heavy hydrogen content ambient atmosphere had many amounts of the amount of deuterium oxide hydrogen water (HDO, D2 O), heavy hydrogen (D2), and deuterium hydrogen (HD) compared with the 1st sample in the condition of not heating so that clearly from drawing 16 and drawing 17 . In addition, H is [heavy hydrogen and O of hydrogen and D] oxygen.
[0086] Analysis of TDS also shows that diffusion of the hydrogen within the PLCSZT ferroelectric film 43 and heavy hydrogen increases with heating in the heavy hydrogen content ambient atmosphere for 20 minutes.
[0087] In addition, analytical method can be measured not only with SIMS and TDS but with an Auger-electron-spectroscopy analysis method (AES) and a hydrogen dispersion front analysis method (HFS).
[0088] By the way, about degradation of the ferroelectric property by the reducing atmosphere, the mechanism is not clear. However, a mechanism as shown in drawing 18 can be considered by this experiment.
[0089] That is, if the 1st or 2nd sample is heated at 200 degrees C in a heavy hydrogen content ambient atmosphere, IrO2 which constitutes the up electrode 44 will be decomposed into Ir and O2 in a vacuum ambient atmosphere, and IrO2 will generate Ir and D2O according to a chemistry reduction operation. Moreover, Ir which constitutes the up electrode 44 functions as a catalyst, and it is D2. 2D+ It changes. Furthermore, Pt layer 42b which constitutes the lower electrode 42 functions as a catalyst, and it is D2. 2D+ It changes. And D+ It is spread on the boundary of electrodes 44 and 42 and the ferroelectric film 43, and, finally enters in the ferroelectric film 43.

[0090] Drawing 19 (a) Capacitor Q0 The model of the perovskite structure immediately after formation is shown, and the titanium (Ti) atom and zirconium (Zr) atom which constitute the PLCSZT ferroelectric film 43 change between the oxygen (O) atoms of the perimeter with change of pulse-voltage E, and produce polarization. On the other hand, D+ When it enters into the PLCSZT ferroelectric film 43, it is drawing 19 (b). It is D+ so that it may be shown. The change of Ti atom or Zr atom is barred, the amount of changes is made small, and the amount Qsw of polarization is reduced.
[0091] by the way -- although ferroelectric film 24a shown in drawing 4 was formed by the spatter with the above-mentioned operation gestalt -- MOCVD -- you may form by law.
[0092] It is common to use the gas containing hydrogen as material gas in formation of the PLCSZT film by the MOCVD method. therefore -- as the result which does not have hydrogen into a membrane formation ambient atmosphere -- as-depo the spatter PLCSZT to which hydrogen does not exist in the film -- differing -- MOCVD -- the PLCSZT film which formed membranes by law -- as-depo Hydrogen exists in the film. The hydrogen concentration in this film is 3 1x1019 pieces/cm. The concentration after it was good in it being the following and the dehydrogenation was carried out by annealing etc. is 3 1x1019 pieces/cm. The hydrogen concentration in PLCSZT in a good and final ferroelectric capacitor is 3 1x1019 pieces/cm with it being the following. It is good in it being the following. It is also the same as when forming the PZT system ingredient film instead of the PLCSZT film.
[0093] The conditions which form the PZT film by the MOCVD method set for example, substrate temperature as 600 degrees C, and are THM about flow rate 0.4 ml/min and Zr (DPM)4 in Pb (DPM)4 as material gas further considering flow rate 0.2 ml/min and Ti (DPM)4 as flow rate 0.2 ml/min and a solvent. The pressure of a sink and its ambient atmosphere is set to 500Pa into a growth ambient atmosphere by flow rate 0.4 ml/min.
[0094] Even in this case, the reduction element concentration in ferroelectric film 24a which forms the ferroelectric film capacitor Q for an MOS transistor on a wrap insulator layer, forms an interlayer insulation film, wiring, and the covering film further, and finally constitutes Capacitor Q is 3 1x1019 pieces/cm the same with having described above. It sets up so that it may become the following.
(1) The concentration of the particle which is formed of CVD on the insulator layer formed on the semi-conductor substrate, the 1st electrode of the capacitor formed on said insulator layer, and said 1st electrode, and has a reduction operation is 3 1x1019 pieces/cm. Semiconductor device characterized by having the ferroelectric film for said capacitors which is the following, and the 2nd electrode of said capacitor formed on said ferroelectric film.
(2) Said particle is a semiconductor device given in the additional remark 1 characterized by being a hydrogen atom or a heavy hydrogen atom at least.
(3) Said ferroelectric is a semiconductor device given in the additional remark 1 or additional remark 2 characterized by being a PZT system ingredient or Bi layer structure compound ingredient.
(4) The process which forms the 1st electrode of a capacitor through an insulator layer on a semi-conductor substrate, The process which forms the ferroelectric film of said capacitor with a CVD method on said 1st electrode, In the manufacture approach of a semiconductor device of having the process which forms the 2nd electrode of said capacitor on said ferroelectric film, and the process which forms the film above said capacitor, at the process after forming said ferroelectric film It is the concentration of a particle with the reduction operation in said ferroelectric film 1x1019 pieces/cm 3 The manufacture approach of the semiconductor device characterized by making it the following.
(5) The process which forms a transistor in a semi-conductor substrate, and the process which forms the 1st electrode of a capacitor through an insulator layer on said semi-conductor substrate, In the manufacture approach of a semiconductor device of having the process which forms the ferroelectric film of said capacitor on said 1st electrode, the process which forms the 2nd electrode of said capacitor on said ferroelectric film, and the process which forms the film above said capacitor The concentration of the particle which has the reduction operation in said ferroelectric film at the process after forming said capacitor is 3 1x1019 pieces/cm. On the

conditions which become the following The manufacture approach of the semiconductor device characterized by having the process which heats said semi-conductor substrate in a hydrogen content ambient atmosphere in order to improve the property of said transistor.
(6) Said particle is the manufacture approach of a semiconductor device given in the additional remark 5 characterized by being a hydrogen atom or a heavy hydrogen atom at least.
(7) Said ferroelectric film is the manufacture approach of a semiconductor device given in the additional remark 5 or additional remark 6 characterized by being formed of a spatter or MOCVD.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing 1 is the sectional view (the 1) showing the formation process of the semiconductor device concerning the operation gestalt of this invention.
[Drawing 2] Drawing 2 is the sectional view (the 2) showing the formation process of the semiconductor device concerning the operation gestalt of this invention.
[Drawing 3] Drawing 3 is the sectional view (the 3) showing the formation process of the semiconductor device concerning the operation gestalt of this invention.
[Drawing 4] Drawing 4 is the sectional view (the 4) showing the formation process of the semiconductor device concerning the operation gestalt of this invention.
[Drawing 5] Drawing 5 is the sectional view (the 5) showing the formation process of the semiconductor device concerning the operation gestalt of this invention.
[Drawing 6] Drawing 6 is the sectional view (the 6) showing the formation process of the semiconductor device concerning the operation gestalt of this invention.
[Drawing 7] Drawing 7 is the sectional view (the 7) showing the formation process of the semiconductor device concerning the operation gestalt of this invention.
[Drawing 8] Drawing 8 is the sectional view (the 8) showing the formation process of the semiconductor device concerning the operation gestalt of this invention.
[Drawing 9] Drawing 9 is the sectional view (the 9) showing the formation process of the semiconductor device concerning the operation gestalt of this invention.
[Drawing 10] Drawing 10 is the sectional view showing other formation processes of the semiconductor device concerning the operation gestalt of this invention.
[Drawing 11] Drawing 11 is the sectional view showing the sample of the ferroelectric capacitor which constitutes the semiconductor device concerning the operation gestalt of this invention.
[Drawing 12] Drawing 12 is heavy hydrogen concentration distribution by the SIMS analysis after carrying out heavy hydrogen processing of the capacitor of the semiconductor device concerning the operation gestalt of this invention.
[Drawing 13] Drawing 13 is heavy hydrogen concentration distribution by the SIMS analysis after carrying out heavy hydrogen processing of the capacitor boundary region of the semiconductor device concerning the operation gestalt of this invention.
[Drawing 14] Drawing 14 is drawing showing the heavy hydrogen processing time of the capacitor of the semiconductor device concerning the operation gestalt of this invention, and the ferroelectric film of the boundary region, and the relation of heavy hydrogen concentration.
[Drawing 15] Drawing 15 is drawing showing the electrical-potential-difference-polarization property of the ferroelectric capacitor by which changed time amount and heavy hydrogen processing was carried out.
[Drawing 16] Drawing 16 is drawing showing the concentration distribution by the TSD analysis of the oxygen in early stages of a ferroelectric capacitor, hydrogen, and heavy hydrogen.
[Drawing 17] Drawing 17 is D2 of a ferroelectric capacitor. It is drawing showing the concentration distribution by the TSD analysis of the oxygen after heating, hydrogen, and heavy hydrogen.
[Drawing 18] Drawing 18 is D2 of a capacitor which has IrO2 and PZT. It is the mechanism of

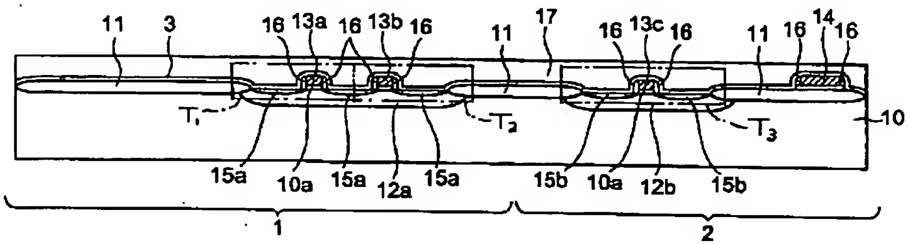
degradation to depend.
[Drawing 19] Drawing 19 (a) and (b) The early stages of the capacitor of a semiconductor device and D2 concerning this invention The ferroelectric film configuration atom condition after heating is shown.
[Description of Notations]
10 -- A semi-conductor substrate, 11 -- An isolation insulator layer, 12a, 12b -- Well field, 13a, 13b, 13c -- A gate electrode, 15a, 15b -- Impurity diffused layer, 16 -- A sidewall, 17, 26, 31, 33, 18a-18e -- Plug, 21 [-- Ferroelectric film,] -- The SiON film, 22 -- SiO2 film, 23a, 25a -- The electric conduction film, 24a 23 [-- Partial wiring, 32a / -- Partial wiring, 32b-32g / -- Wiring, 35 / -- A plug, 36 / -- 37 Aluminum wiring, 38 / -- Covering film.] -- A lower electrode, 24 -- A dielectric film, 25 -- An up electrode, 27

[Translation done.]

DRAWINGS

[Drawing 1]

本発明の実施形態に係る半導体装置の形成工程を示す断面図（その１）

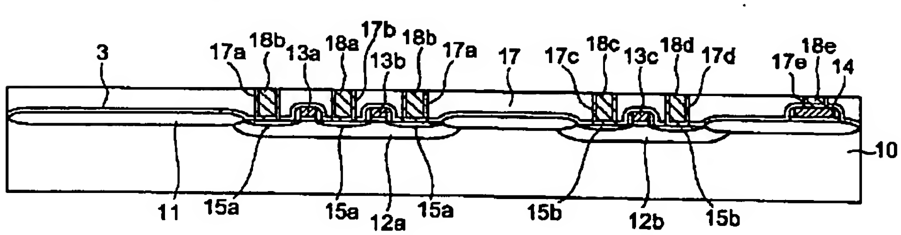


10：半導体基板
12a,12b：ウエル領域
17：層間絶縁膜
11：素子分離絶縁膜
10a：ゲート絶縁膜
13a～13c：ゲート電極

14：配線
15a：n型不純物拡散領域
15b：p型不純物拡散領域
16：側壁絶縁膜
3：カバー膜
Ｔ１～Ｔ３：ＭＯＳトランジスタ

[Drawing 2]

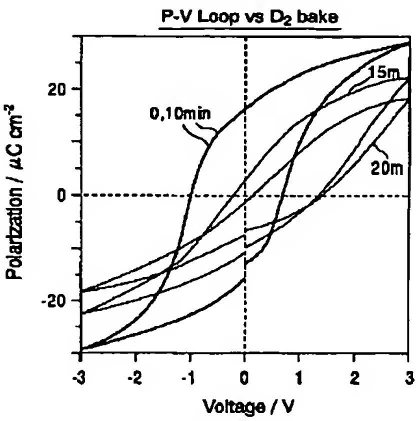
本発明の実施形態に係る半導体装置の形成工程を示す断面図（その２）



１７ａ～１７ｄ：コンタクトホール
１７ｅ：ビアホール
１８ａ～１８ｃ：プラグ

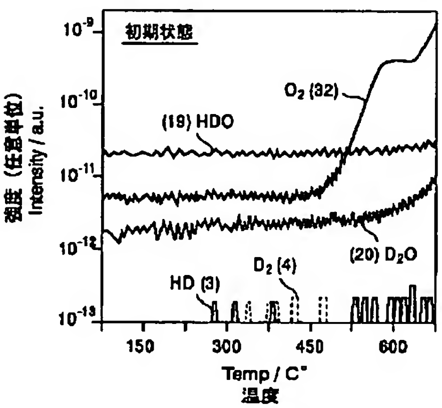
[Drawing 15]

時間を変えて重水素処理された強誘電体
キャパシタの電圧－分極特性



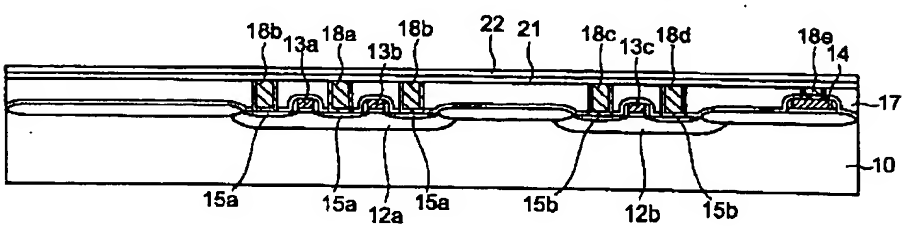
[Drawing 16]

強誘電体キャパシタ初期の酸素、水素、
重水素についてのTSD分析による濃度分布



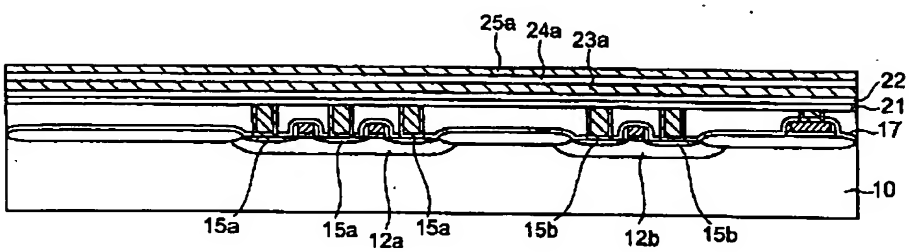
[Drawing 3]

本発明の実施形態に係る半導体装置の形成工程を示す断面図（その３）



[Drawing 4]

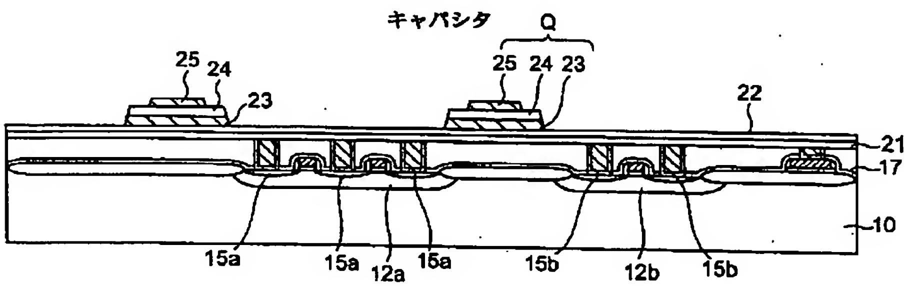
本発明の実施形態に係る半導体装置の形成工程を示す断面図（その４）



２３ａ：第１導電体膜
２４ａ：強誘電体膜
２５ａ：第２導電体膜

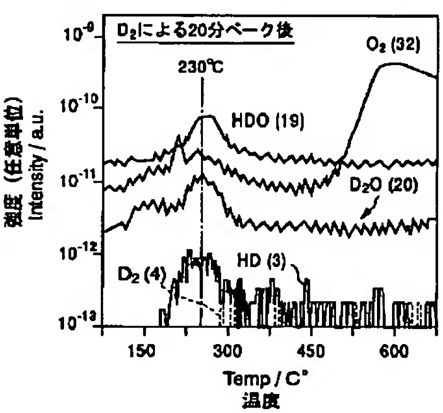
[Drawing 5]

本発明の実施形態に係る半導体装置の形成工程を示す断面図（その５）



[Drawing 17]

強誘電体キャパシタのD_2加熱後の酸素、水素、重水素についてのTSD分析による濃度分布



[Drawing 18]

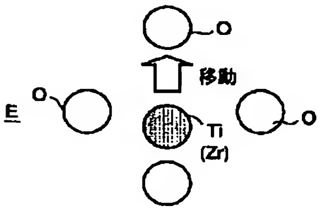
IrO_2とPZTを有するキャパシタのD_2による劣化のメカニズム

1. $IrO_2 \rightarrow Ir+O_2$ (真空還元、副次的)
2. $IrO_2+D_2 \rightarrow Ir+D_2O$ (化学還元)
3. $Ir+D_2 \rightarrow 2D^+(Ir)$ (上部電極触媒反応：主的)
4. $Pt+D_2 \rightarrow 2D^+(Ir)$(下部電極触媒反応：主的)
5. $D^+ + PZT \rightarrow PZT\text{-}D$ (境界拡散及びQ_{SW}低減)

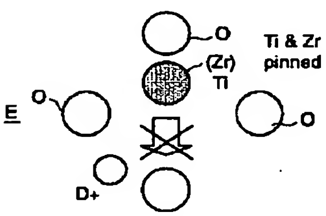
[Drawing 19]

本発明に係る半導体装置のキャパシタの
初期とD_2加熱後の強誘電体構成電子状態

(a) 初期のPZTのペロブスカイト構造

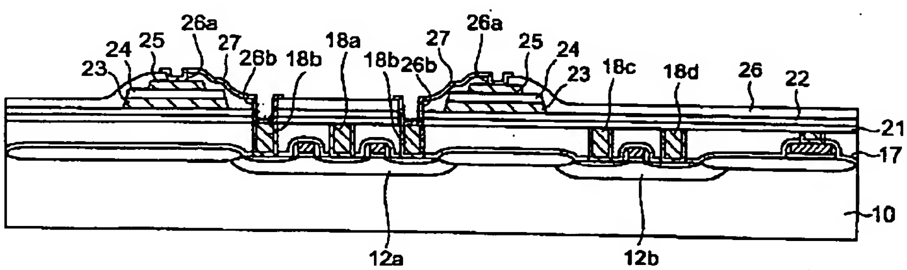


(b)



[Drawing 6]

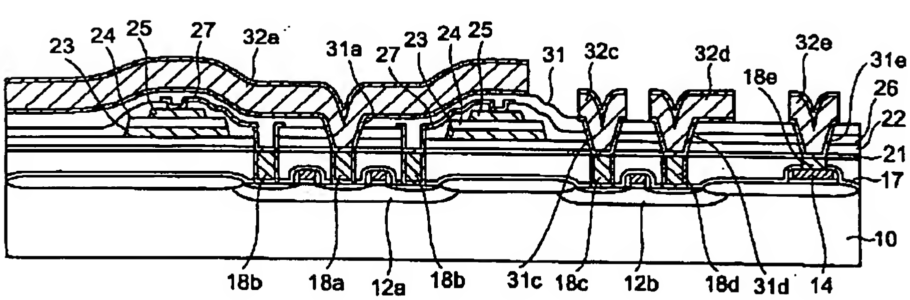
本発明の実施形態に係る半導体装置の形成工程を示す断面図（その６）



２６：層間絶縁膜
２７：局所配線

[Drawing 7]

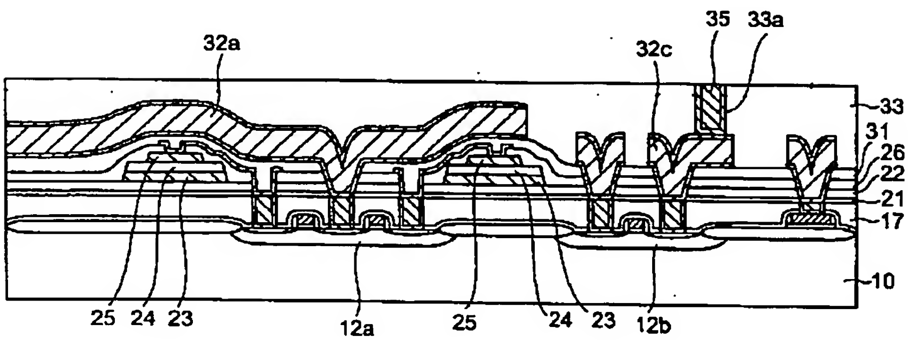
本発明の実施形態に係る半導体装置の形成工程を示す断面図（その７）



３２ａ：ビット線
３２ｂ～３２ｅ：配線

[Drawing 8]

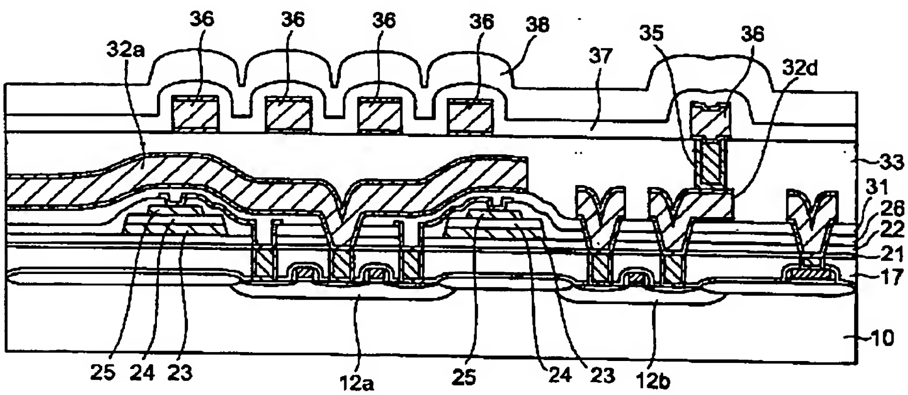
本発明の実施形態に係る半導体装置の形成工程を示す断面図（その８）



３３：層間絶縁膜

[Drawing 9]

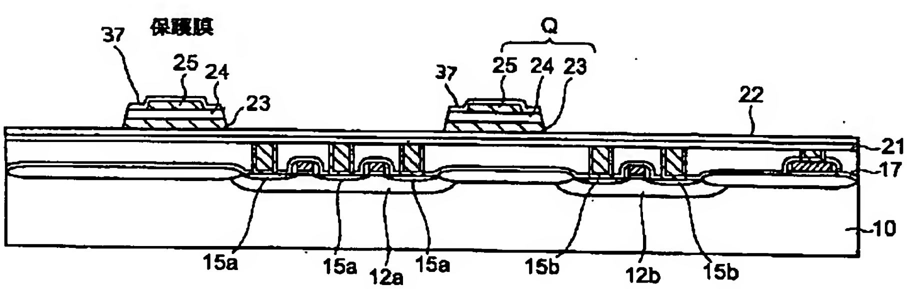
本発明の実施形態に係る半導体装置の形成工程を示す断面図（その９）



３６：配線
３７，３８：カバー膜

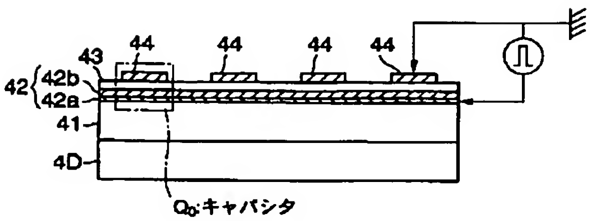
[Drawing 10]

本発明の実施形態に係る半導体装置の他の形成工程を示す断面図



[Drawing 11]

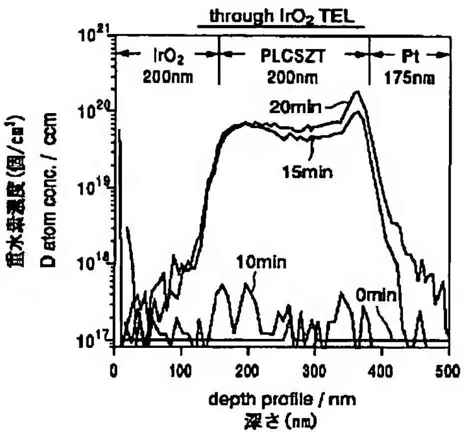
本発明の実施形態に係る半導体装置
を構成する強誘電体キャパシタ



42:下部電極
43:強誘電体膜
44:上部電極

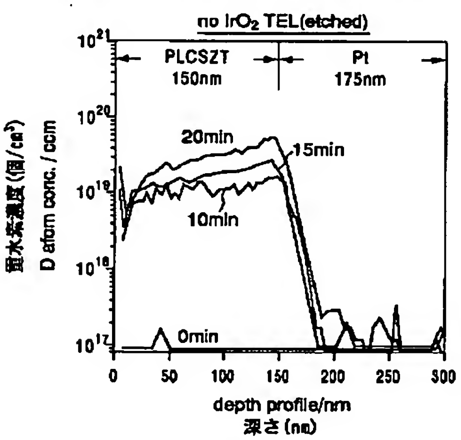
[Drawing 12]

本発明の実施形態に係る半導体装置のキャパシタを
重水素処理した後のSIMS分析による重水素濃度分布



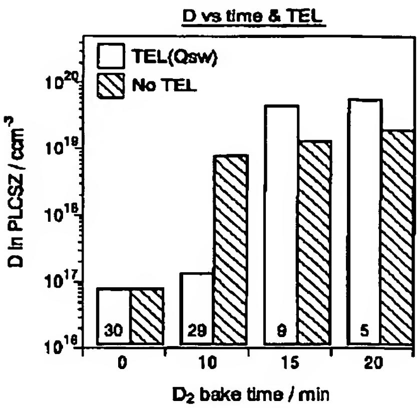
[Drawing 13]

本発明の実施形態に係る半導体装置のキャパシタ周辺領域を
重水素処理した後のSIMS分析による重水素濃度分布



[Drawing 14]

本発明の実施形態に係る半導体装置のキャパシタ及びその
周辺領域の強誘電体膜の重水素処理時間と重水素濃度の関係



[Translation done.]

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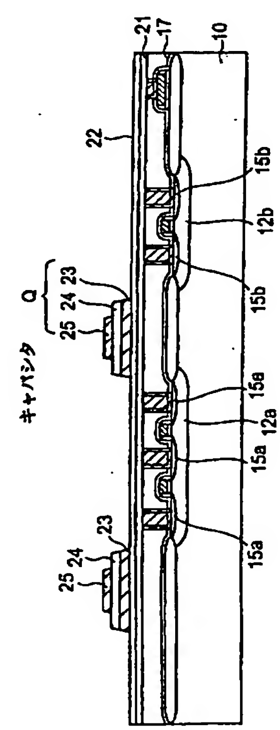
最終頁に続く

(54)【発明の名称】半導体装置及びその製造方法

(57)【要約】
【課題】強誘電体キャパシタを有する半導体装置に関し、強誘電体キャパシタの特性の劣化を抑制すること。
【解決手段】半導体基板１０上に形成された絶縁膜２２と、絶縁膜２２上に形成されたキャパシタＱの第１電極２３と、第１電極２３の上にＭＯＣＶＤ法で形成され且つ還元作用を持つ粒子の濃度が１×１０¹⁹個／cm³ 未満である強誘電体膜２４と、強誘電体膜２４の上に形成された前記キャパシタＱの第２電極２５とを含む。

本発明の実施形態に係る半導体装置の形成工程を示す断面図（その５）



【特許請求の範囲】

【請求項１】半導体基板上に形成された絶縁膜と、
前記絶縁膜上に形成されたキャパシタの第１電極と、
前記第１電極上にＣＶＤにより形成され且つ還元作用を持つ粒子の濃度が1×10^{19}個／cm³ 未満である前記キャパシタ用の強誘電体膜と、
前記強誘電体膜の上に形成された前記キャパシタの第２電極とを有することを特徴とする半導体装置。

【請求項２】前記粒子は、少なくとも水素原子と重水素原子のいずれかであることを特徴とする請求項１に記載の半導体装置。

【請求項３】前記強誘電体は、ＰＺＴ系材料又はBi層状構造化合物材料であることを特徴とする請求項１又は請求項２に記載の半導体装置。

【請求項４】半導体基板上に絶縁膜を介してキャパシタの第１電極を形成する工程と、前記キャパシタの強誘電体膜を前記第１電極上にＣＶＤ法により形成する工程と、前記キャパシタの第２電極を前記強誘電体膜上に形成する工程と、前記キャパシタの上方に膜を形成する工程とを有する半導体装置の製造方法において、
前記強誘電体膜を形成した後の工程で、前記強誘電体膜中への還元作用を持つ粒子の濃度を1×10^{19}個／cm³ 未満にすることを特徴とする半導体装置の製造方法。

【請求項５】半導体基板にトランジスタを形成する工程と、前記半導体基板上に絶縁膜を介してキャパシタの第１電極を形成する工程と、前記キャパシタの強誘電体膜を前記第１電極上に形成する工程と、前記キャパシタの第２電極を前記強誘電体膜上に形成する工程と、前記キャパシタの上方に膜を形成する工程とを有する半導体装置の製造方法において、
前記キャパシタを形成した後の工程で、前記強誘電体膜中の還元作用を持つ粒子の濃度が1×10^{19}個／cm³ 未満となる条件で、前記トランジスタの特性を改善するために水素含有雰囲気中で前記半導体基板を加熱する工程を有することを特徴とする半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体装置に関し、より詳しくは、強誘電体キャパシタを有する半導体装置に関する。

【０００２】

【従来の技術】電源を切っても情報を保持でき、しかも省電力で書き込みや読み出しのできるメモリとして、強誘電体不揮発性メモリ（ＦｅＲＡＭ）が注目されている。ＦｅＲＡＭは転送トランジスタと強誘電体キャパシタからなるメモリセルを有している。強誘電体キャパシタは、下部電極と上部電極により強誘電体膜を挟んだ構造を有している。

【０００３】強誘電体キャパシタを構成する強誘電体膜は、チタン酸ジルコン酸鉛（ＰＺＴ）、LaドープＰＺＴ（ＰＬＺＴ）等のＰＺＴ系材料や、$SrBi_2Ta_2O_9$（ＳＢＴ、Ｙ１）、$SrBi_2(Ta, Nb)_2O_9$（ＳＢＴＮ、ＹＺ）等のBi層状構造化合物材料等があり、それらの材料は、ゾルゲル法、スパッタ法、ＭＯＣＶＤ法等によって成膜される。

【０００４】通常、強誘電体膜は、下部電極上にアモルファス相の強誘電体膜を形成した後に、熱処理によって強誘電体膜をペロブスカイト構造へと結晶化させる。ついで上部電極を強誘電体膜上に形成してキャパシタ構造を得る。

【０００５】上部電極の材料としてプラチナ（Pt）を用いるのが一般的である。プラチナを用いた上部電極はリーク電流が小さく、キャパシタの分極特性のヒステリシスカーブを大きくできるなどの利点があるが、疲労特性が悪いこと、半導体デバイスを作る過程での劣化が大きいこと、信頼性が悪いことが知られている。そのようなPt上部電極については例えば1998年秋（59回）応物29a-K-4 に記載がある。

【０００６】Pt上部電極の問題点を解決するために、IrO_2や$SrRuO_3$（ＳＲＯ）などの酸化導電材を用いた上部電極の開発が行われている。IrO_2から上部電極を形成することについては、例えばISIF 2000, 12th International Symposium on IntergratedFerroelectrics Nop.017C に記載がある。また、ＳＲＯよりなる上部電極を用いることについては、例えば1999年春（60回）応物2p-A-6に記載がある。

【０００７】それらIrO_2、ＳＲＯのような導電性酸化物材料よりなる電極を用いることにより、疲労特性、劣化を抑制して信頼性を改善することができる。

【０００８】一方、還元雰囲気、特に水素原子が強誘電体の特性を劣化させることはよく知られている。そのため、強誘電体と水素を接触させないようにして半導体装置を形成する方法が採られてきた。例えばK. Kushida-A., J. Appl. Phys,. 85, 1069, 1999 には、上部電極上に形成されたPbO 膜によって上部電極を透過する水素の強誘電体膜への拡散を防ぐことが報告されている。

【０００９】また、特許第３１５７７３４号公報では、強誘電体と層間膜の間に水を通さないTiO 等の膜を形成して強誘電体への水素の拡散を防いでいる。

【００１０】さらに、特開平8-37282 号公報では、層間膜中の水素原子濃度を10×10^{21}個／cm³ 以下にすることで、水素原子に起因する強誘電体膜の劣化を抑制できることが示されている。

【００１１】

【発明が解決しようとする課題】しかし、強誘電体キャパシタの還元を防止するために従来採用されている種々の構造は、半導体装置製造の工程を増やすものであったり、或いは過剰に水素工程を避けることによってキャパシタ以外の素子特性の改善が図れなくなることがある。

【００１２】本発明の目的は、強誘電体キャパシタ特性

の劣化を抑制できる半導体装置及びその製造方法を提供することにある。

【００１３】

【課題を解決するための手段】上記した課題は、半導体基板上に形成された絶縁膜と、前記絶縁膜上に形成されたキャパシタの第１電極と、前記第１電極上にＣＶＤにより形成され且つ還元作用を持つ粒子の濃度が１×１０^{19}個／cm^3 未満である前記キャパシタ用の強誘電体膜と、前記強誘電体膜の上に形成された前記キャパシタの第２電極とを有することを特徴とする半導体装置によって解決される。

【００１４】また、上記した課題は、半導体基板上に絶縁膜を介してキャパシタの第１電極を形成する工程と、前記キャパシタの強誘電体膜を前記第１電極上にＣＶＤ法により形成する工程と、前記キャパシタの第２電極を前記強誘電体膜上に形成する工程と、前記キャパシタの上方に膜を形成する工程とを有する半導体装置の製造方法において、前記強誘電体膜を形成した後の工程で、前記強誘電体膜中の還元作用を持つ粒子の濃度を１×１０^{19}個／cm^3 未満にすることを特徴とする半導体装置の製造方法によって解決される。

【００１５】また、上記した課題は、半導体基板にトランジスタを形成する工程と、前記半導体基板上に絶縁膜を介してキャパシタの第１電極を形成する工程と、前記キャパシタの強誘電体膜を前記第１電極上に形成する工程と、前記キャパシタの第２電極を前記強誘電体膜上に形成する工程と、前記キャパシタの上方に膜を形成する工程とを有する半導体装置の製造方法において、前記キャパシタを形成した後の工程で、前記強誘電体膜中の還元作用を持つ粒子の濃度が１×１０^{19}個／cm^{3}未満となる条件で、前記トランジスタの特性を改善するために水素含有雰囲気中で前記半導体基板を加熱する工程を有することを特徴とする半導体装置の製造方法によって解決される。

【００１６】本発明によれば、強誘電体膜中の還元作用を持つ粒子の濃度、例えば水素原子と重水素原子の濃度の総和を１×１０^{19}個／cm^3 未満としたので、水素、重水素等に起因する強誘電体の劣化を防いで強誘電体キャパシタの特性を抑制できことが実験により明らかになった。

【００１７】また、水素原子と重水素原子の総和を１×１０^{17}個／cm^3 未満とすることにより、さらにキャパシタ特性の劣化を防止することができる。

【００１８】

【発明の実施の形態】以下に本発明の実施形態を図面に基づいて説明する。

【００１９】図１～図１６は本発明の一実施形態の半導体装置の製造方法を工程順に示す断面図である。なお、本実施形態の半導体装置としてＦｅＲＡＭを例に挙げて説明する。

【００２０】まず、図１に示す断面構造を得るまでの工程を説明する。

【００２１】図１に示すように、ｐ型シリコン（半導体）基板１０表面に、ＬＯＣＯＳ（Local Oxidation of Silicon）法により素子分離絶縁膜１１を選択的に形成する。素子分離絶縁膜１１としてSTI（Shallow Trench Isolation）を採用してもよい。

【００２２】続いて、シリコン基板１０のメモリセル領域１、周辺回路領域２における所定の活性領域（トランジスタ形成領域）にｐ型不純物及びｎ型不純物を選択的に導入して、ｐウェル１２ａ及びｎウェル１２ｂを形成する。なお、図１には示していないが、周辺回路領域２ではＣＭＯＳを形成するためにｐウェル（不図示）も形成される。

【００２３】その後、シリコン基板１０の活性領域表面を熱酸化して、ゲート絶縁膜１０ａとしてシリコン酸化膜を形成する。

【００２４】次に、シリコン基板１０の上側全面にアモルファスシリコン膜及びタングステンシリサイド膜を順次形成し、これらのアモルファスシリコン膜及びタングステンシリサイド膜をフォトリソグラフィ法により所定の形状にパターニングして、ゲート電極１３ａ～１３ｃ及び配線１４を形成する。なお、ゲート電極１３ａ～１３ｃを構成するアモルファスシリコン膜の代わりにポリシリコン膜を形成してもよい。

【００２５】メモリセル領域１では、１つのｐウェル１２ａ上には２つのゲート電極１３ａ，１３ｂが並列に配置され、それらのゲート電極１３ａ、１３ｂはワード線ＷＬの一部を構成する。

【００２６】次に、メモリセル領域１において、ゲート電極１３ａ，１３ｂの両側のｐウェル１２ａ内にｎ型不純物をイオン注入して、ｎチャネルＭＯＳトランジスタのソース・ドレインとなるｎ型不純物拡散領域１５ａを形成する。これと同時に、周辺回路領域２のｐウェル（不図示）にもｎ型不純物拡散領域を形成してもよい。続いて、周辺回路領域２において、ゲート電極１３ｃの両側のｎウェル１２ｂにｐ型不純物をイオン注入して、ｐチャネルＭＯＳトランジスタのソース・ドレインとなるｐ型不純物拡散領域１５ｂを形成する。ｎ型不純物とｐ型不純物の打ち分けは、レジストパターンを使用して行われる。

【００２７】その後に、シリコン基板１０の全面に絶縁膜を形成した後、その絶縁膜をエッチバックしてゲート電極１３ａ～１３ｃ及び配線１４の両側部分に側壁絶縁膜１６として残す。その絶縁膜として、例えばＣＶＤ（化学気相成長）法により酸化シリコン（SiO_2）を形成する。

【００２８】さらに、ゲート電極１３ａ，１３ｂと側壁絶縁膜１６をマスクに使用して、メモリセル領域１のｎ型不純物拡散領域１５ａ内に再びｎ型不純物をイオン注

入することにより、ｎ型不純物拡散領域１５ａをＬＤＤ構造にする。これと同時に周辺回路領域２におけるｎ型不純物拡散領域１５ａもＬＤＤ構造にする。また、周辺回路領域２におけるｐ型不純物拡散領域１５ｂ内に再びｐ型不純物をイオン注入することにより、ｐ型不純物拡散領域をＬＤＤ構造にする。

【００２９】以上の工程により、ｐウェル１２ａにはゲート電極１３ａ，１３ｂとＬＤＤ構造のｎ型不純物拡散層１５ａを有する２つのＭＯＳトランジスタT_1、T_2が形成される。また、ｎウェル１２ｂにはゲート電極１３ｃとＬＤＤ構造のｐ型不純物拡散層１５ｂを有するＭＯＳトランジスタT_3が形成される。

【００３０】次に、ＭＯＳトランジスタを覆うカバー膜として約２００ｎｍの厚さの酸窒化シリコン（SiON）膜をプラズマＣＶＤ法によりシリコン基板１０の全面に形成する。その後、ＴＥＯＳガスを用いるプラズマＣＶＤ法により、第１の層間絶縁膜１７として膜厚１．０μｍ程度の酸化シリコン（SiO_2）をカバー膜３の上に成長させる。

【００３１】続いて、第１の層間絶縁膜１７の緻密化処理として、例えば常圧の窒素雰囲気中で第１の層間絶縁膜１７を７００℃の温度で３０分間熱処理する。その後に、第１の層間絶縁膜１７の上面を化学的機械研磨（ＣＭＰ）法により平坦化する。

【００３２】次に、図２に示す構造を形成するまでの工程を説明する。

【００３３】まず、フォトリソグラフィ法によりカバー膜３と第１層間絶縁膜１７をパターニングして、不純物拡散領域１５ａ，１５ｂに到達する深さのコンタクトホール１７ａ～１７ｄと、配線１４に到達する深さのビアホール１７ｅをそれぞれ第１の層間絶縁膜１７に形成する。その後、第１の層間絶縁膜１７上面とホール１７ａ～１７ｅ内面に膜厚２０ｎｍのTi（チタン）薄膜と膜厚５０ｎｍのTiN（チタンナイトライド）薄膜をスパッタ法により順に形成する。さらに、ＣＶＤ法によりタングステン（W）をTiN薄膜上に成長する。これにより、コンタクトホール１７ａ～１７ｄ、ビアホール１７ｅ内にタングステン膜が埋め込まれた状態となる。

【００３４】その後、第１の層間絶縁膜１７上面が露出するまでタングステン膜、ＴｉＮ薄膜及びＴｉ薄膜をＣＭＰ法により研磨する。これによりホール１７ａ～１７ｅ内に残されたチタン膜、窒化チタン膜及びタングステン膜は、それぞれ導電性プラグ１８ａ～１８ｅとして使用される。

【００３５】メモリセル領域１の１つのｐウェル１２ａにおいて２つのゲート電極１３ａ，１３ｂに挟まれるｎ型不純物拡散領域１５ａ上の第１の導電性プラグ１８ａは後述するビット線に接続され、さらに、残り２つの第２の導電性プラグ１８ｂは後述するキャパシタに接続される。

【００３６】次に、図３に示すように、シランとアンモニアを用いるプラズマＣＶＤ法により、第１の層間絶縁膜１７上と導電性プラグ１８ａ～１８ｅの上にSiON（絶縁膜）膜２１を１２０ｎｍの厚さに形成する。このSiON膜２１は、導電性プラグ１８ａ～１８ｅの酸化を防止するために形成される。さらに、反応ガスとしてＴＥＯＳと酸素を用いるプラズマＣＶＤ法により厚さ１５０ｎｍのSiO_2膜２２をSiON膜２１上に形成する。なお、SiO_2膜２２は、第１の層間絶縁膜１７への水の侵入を防止するために形成される。

【００３７】その後、SiON膜２１、SiO_2膜２２の緻密化のために、それらの膜を例えば常圧の窒素雰囲気中で温度６５０℃で３０分間熱処理する。

【００３８】次に、図４に示すように、ＤＣスパッタ法により、膜厚１０～３０ｎｍのチタンと膜厚１００～３００ｎｍのプラチナをSiO_2膜２２上に純に形成して二層構造の第１導電膜を形成する。なお、第１の導電膜２３ａとして、イリジウム、ルテニウム、酸化ルテニウム、酸化イリジウム、酸化ルテニウムストロンチウム($SrRuO_3$)等の膜を形成してもよい。

【００３９】続いて、ＲＦスパッタ法により、第１の導電膜２３ａの上に強誘電体膜２４ａとして、ランタン・カルシウム・ストロンチウムドープトチタン酸ジルコン酸鉛（ＰＬＣＳＺＴ）膜をスパッタ法により１００～３００ｎｍ、例えば２００ｎｍの厚さに形成する。

【００４０】スパッタ条件は、ターゲットとして焼結したＰＬＣＳＺＴを用い、Arガスを用い、１．0Pa、ＲＦパワー１kWである。この処理中にはＰＬＣＳＺＴ膜を水素又は重水素中に曝す工程は無く、ＰＬＣＳＺＴ膜中への水素と重水素の混入は考えられない。また、後述するようにアニール後のＰＬＣＳＺＴ膜中の水素と重水素の濃度は1×10^{19}個／cm^3以下であることから、ＰＬＣＳＺＴ膜のas-depo膜中の水素又は重水素の濃度も1×10^{19}個／cm^3以下であることが容易に推定できる。なお、ＰＬＣＳＺＴ膜の代わりにＰＺＴ系材料膜を形成する場合も同様である。

【００４１】続いて、強誘電体膜２４ａの結晶化処理として、酸素雰囲気中で温度６００～８５０℃、３０～１２０秒間の条件でＲＴＡ(Rapid Thermal Annealing)を行う。例えば、温度７５０℃で６０秒間アニールする。

【００４２】強誘電体材料膜の形成方法としては、上記したスパッタ法の他にスピンオン法、ゾル－ゲル法、ＭＯＤ(Metal Organi Deposition)法、ＭＯＣＶＤ（有機金属ＣＶＤ）法があり、ＭＯＣＶＤ法については後述する。

【００４３】強誘電体膜２４ａの材料としてはＰＬＣＳＺＴの他に、ＰＺＴ、ＰＬＺＴのような他のＰＺＴ系材料や、$SrBi_2Ta_2O_9$、$SrBi_2(Ta、Nb)_2O_9$等のBi層状構造化合物材料、その他の金属酸化物強誘電体であってもよい。

【００４４】そのような強誘電体膜２４ａを形成した後に、その上に第２の導電膜２５ａとして酸化イリジウム(IrO_2)膜をスパッタ法により１００～３００ｎｍの厚さに形成する。なお、第２の導電膜２５ａとして、Pt膜もしくはＳＲＯ膜をスパッタ法により形成してもよい。

【００４５】次に、第２の導電膜２５ａの上にレジストを塗布し、さらにレジストを露光、現像して上部電極形状にパターニングする。その後に、レジストパターンをマスクに使用して第２の導電膜２５ａをドライエッチングして、第２の導電膜２５ａをキャパシタの上部電極２５にする。この後に、レジストを酸素プラズマによりアッシングして除去する。

【００４６】次に、上部電極２５のパターン形成によりダメージを受けた強誘電体膜２４ａを酸素雰囲気中で６５０℃、６０分の条件でアニールし、これにより強誘電体膜の膜質を改善する。これによる強誘電体膜２４ａ中の還元作用を持つ粒子、例えば水素、重水素等の粒子の濃度は1×10^{11}個／cm^3 未満である。

【００４７】この後に、Al_2O_3 よりなる保護膜を上部電極２５、強誘電体膜２４ａの上に形成してもよいが、スパッタ法により強誘電体膜２４ａを形成する場合には省略する。

【００４８】続いて、強誘電体２４ａ及び第１の導電膜２３ａをフォトリソグラフィ法により順次パターニングする。なお、第１の導電膜２３ａをパターニングした後に、酸素含有雰囲気内で温度６５０℃で６０分間加熱して強誘電体膜２４ａの膜質を改善する。

【００４９】これにより、強誘電体膜２４ａはキャパシタ用の誘電体膜２４となり、第１の導電膜２３ａはキャパシタ用の下部電極２３となる。そして、上部電極２５、誘電体膜２４及び下部電極２３によりキャパシタＱが構成される。

【００５０】以上のような工程を経てキャパシタＱを形成した後に、図６に示すように、全面にSiO_2膜及びＳＯＧ膜からなる２層構造の第２の層間絶縁膜２６を形成し、この第２の層間絶縁膜２６によりキャパシタＱを覆う。そのSiO_2膜は、ＴＥＯＳガスを用いるプラズマＣＶＤ法により、成長温度が３９０℃、パワーが４００Ｗの条件でシリコン基板１０の上側全面に１００～３００ｎｍの厚さで形成される。また、ＳＯＧ膜は、ＴＥＯＳ膜上にＳＯＧ溶液を８０～２００ｎｍの厚さに塗布した後に、これを加熱することにより形成される。

【００５１】そして、フォトリソグラフィ法により第２の層間絶縁膜２６をパターニングして、キャパシタＱの上部電極２５の上にコンタクトホール２６ａを形成する。その後、誘電体膜２４に対して回復アニールを実施する。具体的には、酸素雰囲気中で５００～６５０℃の温度で３０～１２０分間加熱する。

【００５２】次に、第２の層間絶縁膜２６、SiON膜２１、SiO_2膜２２をフォトリソグラフィ法によりパターニングして、メモリセル領域１の第２の導電性プラグ１８ｂの上にコンタクトホール２６ｂを形成して第２の導電性プラグ１８ｂを露出させる。そして、第２の層間絶縁膜２６上とコンタクトホール２６ａ，２６ｂ内に、膜厚１００ｎｍのTiN 膜をスパッタ法により形成する。続いて、そのTiN 膜をフォトリソグラフィ法でパターニングすることにより、メモリセル領域１においてコンタクトホール２６ａ，２６ｂを通してｐウェル１２ａ上の第２の導電性プラグ１８ｂとキャパシタ上部電極２５とを電気的接続するための局所配線（ローカル配線）２７を形成する。

【００５３】次に、図７に示すような構造を形成するまでの工程を説明する。

【００５４】まず、局所配線２７と第２の層間絶縁膜２６の上に、プラズマＣＶＤ法によりＴＥＯＳ膜を２００～４００ｎｍの厚さに形成する。このＴＥＯＳ膜は第３の層間絶縁膜３１として使用される。

【００５５】続いて、メモリセル領域１における第３の層間絶縁膜３１からその下方のSiON膜２１までをフォトリソグラフィ法によりパターニングすることにより、ｐウェル１２ａの中央位置の第１の導電性プラグ１８ａの上にコンタクトホール３１ａを形成するとともに、周辺回路領域２の各導電性プラグ１８ｃ～１８ｅ上にもコンタクトホール３１ｃ～３１ｅを形成する。

【００５６】さらに、第３の層間絶縁膜３１の上とコンタクトホール３１ｃ～３１ｅの中にTi膜，TiN 膜、Al（アルミニウム）膜及びTiN 膜の４層を順次積層し、これらの金属膜をパターニングすることにより、メモリセル領域１でビット線３２ａを形成するとともに、周辺回路領域２では配線３２ｃ～３２ｅを形成する。これらのビット線３２ａ、配線３２ｃ～３２ｅは、一層目のアルミニウム配線となる。

【００５７】なお、メモリセル領域１のビット線３２ａは第１の導電性プラグ１８ａに接続され、また、周辺回路領域２の配線３２ｃ～３２ｅは各導電性プラグ１８ｃ～１８ｅに接続される。

【００５８】ビット線３２ａ、配線３２ｃ～３２ｅを構成する各金属膜の膜厚として例えば最下層のTi膜を２０ｎｍの厚さ、下側のTiN 膜を５０ｎｍの厚さ、Al膜を５００ｎｍの厚さ、上側のTiN 膜を１００ｎｍの厚さとする。

【００５９】次に、図８に示すような構造を形成するまでの工程を説明する。

【００６０】まず、ＴＥＯＳガスと酸素(O_2)ガスを使用するプラズマＣＶＤ法により、２．０μｍの厚さのSiO_2からなる第４の層間絶縁膜３３を第３の層間絶縁膜３１、ビット線３２ａ及び配線３２ｃ～３２ｅの上に形成する。

【００６１】さらに、第４の層間絶縁膜３３の上面をＣＭＰ法により研磨して平坦化する。その研磨量は、最上

面から約１．０μmの厚さ相当程度とする。

【００６２】さらに、フォトリソグラフィ法により第４の層間絶縁膜３３をパターニングして、一層目のアルミニウム配線、例えば周辺回路領域２の配線３２ｄに到達するビアホール３３ａを形成する。

【００６３】続いて、ビアホール３３ａの内面と第４の層間絶縁膜３３の上面に、膜厚２０ｎｍのＴｉ膜と膜厚５０ｎｍのＴｉＮ膜をスパッタリングにより順次形成し、それらの膜をグルーレイヤ３５ａとする。その後、グルーレイヤ３５ａ上にタングステン膜３５ｂを形成する。これにより、ビアホール３３ａ内には、グルーレイヤ３５ａとタングステン膜３５ｂが充填される。

【００６４】その後、第４の層間絶縁膜３３上面上のタングステン膜３５ｂ及びグルーレイヤ３５ａをＣＭＰ法又はエッチバックにより除去して、ビアホール３３ａ内にのみ残存させる。

【００６５】次に、図９に示すような構造を形成するまでの工程を説明する。

【００６６】まず、第４の層間絶縁膜３３の上に第１のTiN 膜を５０ｎｍ、Al膜を５００ｎｍ、第２のTiN 膜を５０ｎｍの厚さに順次形成する。続いて、第１及び第２のTiN 膜とAl膜をフォトリソグラフィ法によりパターニングすることにより二層目のアルミニウム配線３６を形成する。

【００６７】続いて、ＴＥＯＳを用いるプラズマＣＶＤ法により、二層目のアルミニウム配線３６と第４の層間絶縁膜３３の上に、第１のカバー絶縁膜３７としてSiO_2膜を２００ｎｍの厚さに形成する。さらに、第１のカバー絶縁膜３７の上に、プラズマＣＶＤ法によりSiN よりなる第２のカバー絶縁膜３８を５００ｎｍの厚さに形成する。これらの第１及び第２のカバー膜３７，３８により二層目の配線３６が被覆される。

【００６８】その後に、ＭＯＳトランジスタT_1，T_2，T_3の特性を向上するために、水素窒素混合ガスの雰囲気中で全体を４００～４５０℃で加熱する。その雰囲気中の水素含有量や加熱温度は、キャパシタＱを構成する強誘電体膜２４ａ中で還元作用を持つ粒子、例えば水素、重水素等の粒子の濃度が最終的に１×10^{19}個／cm^3未満になるような条件に設定する。即ち、強誘電体膜２４ａの形成の初期状態から１×10^{19}個／cm^3 未満までの強誘電体膜２４ａへの還元粒子の侵入は許容される。例えば、キャパシタ誘電体膜２４である強誘電体膜２４ａにおいて、初期状態から１×10^{19}個／cm^3 未満の還元粒子（重水素、水素等）の増加によるキャパシタ特性は問題がない。

【００６９】以上のような実施形態では、キャパシタＱを形成した後の状態において、強誘電体膜２４ａ中で還元作用を持つ粒子の濃度を１×10^{17}個／cm^3 未満とし、キャパシタＱを形成した後からＭＯＳトランジスタT_1，T_2，T_3 の特性改善のための加熱処理を終えた状態で、強誘電体膜２４ａ中の還元作用粒子濃度が１×10^{19}個／cm^3 未満、好ましくは１×10^{17}個／cm^3 未満になるように各工程の条件を調整する。これにより、強誘電体キャパシタの劣化が妨げられる。

【００７０】また、ＭＯＳトランジスタ特性の改善のために水素含有雰囲気中でアニールを終えるまでの工程において、キャパシタＱの強誘電体膜２４ａ中の還元作用原子の濃度が、１×10^{19}個／cm^3 以上になるような場合には、例えば図１０に示すように、上部電極２５のパターンを形成した後に、上部電極２５と強誘電体膜２４ａの上にAl_2O_3 等の金属酸化膜によりなる還元防止用の保護膜３７を形成し、その後に、強誘電体膜２４ａと第１の導電膜２３ａをパターニングする。この保護膜３７は、強誘電体膜２４ａの還元を抑制するために形成される。

【００７１】これにより、水素含有雰囲気中での加熱処理を終えた状態で、その濃度が１×10^{19}個／cm^3 未満になるように調整することが可能である。その他に、層間絶縁膜１７，２６，３３の形成条件やアニール条件を選ぶことにより酸化物強誘電体膜の中の水素濃度を１×10^{19}個／cm^3 未満、好ましくは１×10^{17}個／cm^3未満にして、キャパシタ特性Ｑの劣化を防止する。

【００７２】次に、スパッタ法により形成された強誘電体膜２４ａを有するキャパシタＱの特性がキャパシタＱ形成後の還元雰囲気でどような影響されるかを説明する。

【００７３】まず、図１１に示すように、半導体基板４０上に絶縁膜４１を介してチタン層４２ａとプラチナ層４２ｂの二層構造からなる下部電極４２を形成した後に、下部電極上に膜厚２００ｎｍのＰＬＣＳＺＴ強誘電体膜膜４３をスパッタ法により形成した。そして、ＰＬＣＳＺＴ強誘電体膜４３を常圧の酸素雰囲気中で６００～７５０℃でＲＴＡ処理して膜質を改善した。さらにＰＬＣＳＺＴ強誘電体膜４３上に膜厚２００ｎｍのIr_2O膜をスパッタ法により形成し、これをレジストとエッチングを用いてパターニングし、これによりIr_2O上部電極４４を複数形成し、ついで酸素雰囲気中で６５０℃で加熱した。

【００７４】１つのIr_2O上部電極４４とその下のＰＬＣＳＺＴ強誘電体膜４３及び下部電極４２によって１つのキャパシタQ_0が構成される。

【００７５】そのようなキャパシタQ_0を有する試料として、その上部電極４４の平面形状を５０×５０μm^2の大きさとした第１の試料と、その平面形状を２００×２００μm^2 の大きさとした第２の試料とを作成した。

【００７６】そして、そのような強誘電体キャパシタQ_0を有する第１及び第２の試料を４．５Torrの還元ガス含有雰囲気中で温度２００℃で加熱した。還元ガス含有雰囲気は、３％の重水素（D_2 ）を含む重水素・窒素雰囲気である。ここで重水素は、濃度検出の容易さから水

素の代わりに用いられている。また、加熱時間は、０分、１０分、１５分、２０分と複数設定した。なお、０分の加熱というのは、加熱をしないことを示す。

【００７７】第１及び第２の試料について、二次イオン型質量分析法（ＳＩＭＳ）によって重水素濃度を調べたところ、キャパシタQ_0の部分では上部電極４４の上面からの深さ方向に図１２に示すような重水素濃度分布が存在した。また、キャパシタQ_0の周囲の上部電極４４が形成されていない部分ではＰＬＣＳＺＴ強誘電体膜４３上面から深さ方向に図１３に示すような重水素濃度分布が存在した。なお、図１２、図１３及び以下の図において「Ir_2OＴＥＬ」は上部電極４４が形成された箇所を示し、「no Ir_2O ＴＥＬ」はエッチングにより上部電極４４が除去された箇所を示している。

【００７８】ＳＩＭＳにより試料中の水素濃度を測定する適当な手段が無く、実験方法と趣旨を考慮すれば、重水素の濃度を水素濃度と置き換えて考えても、また、還元作用を持つ粒子の濃度と置き換えても、還元能力の程度を知ることができ、問題はない。

【００７９】図１２及び図１３に基づき、熱時間の違いにより第１及び第２試料のＰＬＣＳＺＴ強誘電体膜中の重水素原子濃度にどのような影響を及ぼすかを棒グラフに表して比較したところ、図１４に示すようになった。

【００８０】図１４中で、「ＴＥＬ」は、ＰＬＣＳＺＴ強誘電体膜４３のうち上部電極４４に覆われた部分のＤ濃度を示し、また、「ＮｏＴＥＬ」は、ＰＬＣＳＺＴ強誘電体膜４３のうち上部電極４４がエッチングされた部分のＤ濃度を示している。

【００８１】図１４によれば、上部電極４４に覆われているＰＬＣＳＺＴ強誘電体膜４３、即ちキャパシタQ_0を構成しているＰＬＣＳＺＴ強誘電体膜４３の中のＤ濃度は１０分程度の重水素・窒素雰囲気での加熱によって殆ど増加していなかった。しかし、上部電極４４に覆われていない部分のＰＬＣＳＺＴ強誘電体膜４３中のＤ濃度は１０分程度の加熱によって8×10^{18}／cm^3程度まで上昇した。

【００８２】さらに、未加熱状態（０分）の第２の試料のキャパシタQ_0と、１０分、１５分、２０分加熱後の第２の試料のキャパシタQ_0のそれぞれに±３Ｖのパルス電圧を印加して電圧・分極特性を調べたところ、図１５に示すような結果が得られた。

【００８３】図１５に示した分極電荷量（Qsw）は、図１４の「ＴＥＬ」のグラフを参照して明らかなように、重水素濃度（Ｄ）が増加するに従って小さくなってくる。本発明者らの実験によれば、重水素濃度が1×10^{19}／cm^3以上になると、ＦｅＲＡＭセルとして書き込み、読み出しにエラーが生じ易い状態になった。ここで、重水素（Ｄ）濃度は水素（Ｈ）濃度に対応していて、還元原子濃度が1×10^{19}／cm^3未満となることが好ましい。

【００８４】次に、１ｃｍ×１ｃｍの大きさの第１の試料について、未加熱状態のものと、重水素含有雰囲気で２０分間加熱されたものについて、それぞれ昇温脱離分析法（ＴＤＳ）によって測定したところ、図１６と図１７に示すような結果が得られた。ＴＤＳの測定は、第１の試料を真空雰囲気中に置くとともに、第１の試料を昇温速度１℃／秒で常温から７５０℃まで昇温して行った。

【００８５】図１６，図１７から明らかなように、重水素含有雰囲気中で２０分間加熱した第１の試料は、未加熱状態の第１の試料に比べて、酸化ジュウテリウム水素水（ＨＤＯ、D_2Ｏ）の量と重水素（D_2）とジュウテリウム水素（ＨＤ）の量が多かった。なお、Ｈは水素、Ｄは重水素、Ｏは酸素である。

【００８６】ＴＤＳの分析によっても２０分間の重水素含有雰囲気での加熱によって、ＰＬＣＳＺＴ強誘電体膜４３内での水素、重水素の拡散が多くなることが分かる。

【００８７】なお、分析方法はＳＩＭＳ、ＴＤＳだけでなく、オージェ電子分光分析法（ＡＥＳ）、水素散乱前方分析法（ＨＦＳ）によっても測定できる。

【００８８】ところで、還元性雰囲気による強誘電体特性の劣化については、そのメカニズムは明確になっていない。しかし、今回の実験により、図１８に示すようなメカニズムが考えられる。

【００８９】即ち、重水素含有雰囲気中で２００℃で第１又は第２の試料を加熱すると、上部電極４４を構成するIrO_2は真空雰囲気中でIrとO_2に分解され、また、IrO_2は化学還元作用によってIrとD_2Oを生成する。また、上部電極４４を構成するIrが触媒として機能してD_2を２Ｄ'に変える。さらに、下部電極４２を構成するPt層４２ｂが触媒として機能してD_2を２Ｄ'に変える。そして、Ｄ'が電極４４，４２と強誘電体膜４３との境界に拡散し、最終的に強誘電体膜４３内に入る。

【００９０】図１９(a) は、キャパシタQ_0形成直後のペロブスカイト構造のモデルを示し、ＰＬＣＳＺＴ強誘電体膜４３を構成するチタン（Ti）原子やジルコニウム（Zr）原子はその周囲の酸素（Ｏ）原子との間をパルス電圧Ｅの変化とともに変移して分極を生じさせる。これに対して、Ｄ'がＰＬＣＳＺＴ強誘電体膜４３中に入り込むと、図１９(b) に示すように、Ｄ'はTi原子やZr原子の変移を妨げてその変移量を小さくして分極量Qswを低減する。

【００９１】ところで、上記した実施形態では、図４に示した強誘電体膜２４ａをスパッタ法により形成したが、ＭＯＣＶＤ法によって形成してもよい。

【００９２】ＭＯＣＶＤ法によるＰＬＣＳＺＴ膜の形成では、水素を含んだガスを原料ガスとして用いるのが一般的である。そのため、成膜雰囲気中に水素がない結果としてas-depo 膜中に水素が存在しないスパッタＰＬＣ

ＳＺＴと異なり、ＭＯＣＶＤ法で成膜したＰＬＣＳＺＴ膜では、as-depo 膜中に水素が存在する。この膜中の水素濃度が1×10^{19}個／ｃｍ^3 以下であるとよく、また、アニール等で脱水素された後の濃度が1×10^{19}個／ｃｍ^3 以下であるとよく、また、最終的な強誘電体キャパシタ中のＰＬＣＳＺＴ中の水素濃度が1×10^{19}個／ｃｍ^3 以下であるとよい。ＰＬＣＳＺＴ膜の代わりにＰＺＴ系材料膜を形成する場合も同様である。

【００９３】ＭＯＣＶＤ法によりＰＺＴ膜を形成する条件は、例えば、基板温度を６００℃に設定し、さらに、原料ガスとして$Pb(DPM)_2$を流量０．４ml/min、$Zr(DPM)_4$を流量０．２ml/min、$Ti(DPM)_4$を流量０．２ml/min 、溶媒としてTHM を流量０．４ml/minで成長雰囲気中に流し、その雰囲気の圧力を５００Paとする。

【００９４】この場合でも、上記したと同様に、ＭＯＳトランジスタを覆う絶縁膜上に強誘電体膜キャパシタＱを形成し、さらに層間絶縁膜、配線、カバー膜を形成し、最終的に、キャパシタＱを構成する強誘電体膜２４ａ内の還元元素濃度が1×10^{19}個／ｃｍ^3 未満になるように設定する。

（１）半導体基板上に形成された絶縁膜と、前記絶縁膜上に形成されたキャパシタの第１電極と、前記第１電極上にＣＶＤにより形成され且つ還元作用を持つ粒子の濃度が1×10^{19}個／cm^3 未満である前記キャパシタ用の強誘電体膜と、前記強誘電体膜の上に形成された前記キャパシタの第２電極とを有することを特徴とする半導体装置。

（２）前記粒子は、少なくとも水素原子と重水素原子のいずれかであることを特徴とする付記１に記載の半導体装置。

（３）前記強誘電体は、ＰＺＴ系材料又はBi層状構造化合物材料であることを特徴とする付記１又は付記２に記載の半導体装置。

（４）半導体基板上に絶縁膜を介してキャパシタの第１電極を形成する工程と、前記キャパシタの強誘電体膜を前記第１電極上にＣＶＤ法により形成する工程と、前記キャパシタの第２電極を前記強誘電体膜上に形成する工程と、前記キャパシタの上方に膜を形成する工程とを有する半導体装置の製造方法において、前記強誘電体膜を形成した後の工程で、前記強誘電体膜中の還元作用を持つ粒子の濃度を1×10^{19}個／cm^3 未満にすることを特徴とする半導体装置の製造方法。

（５）半導体基板にトランジスタを形成する工程と、前記半導体基板上に絶縁膜を介してキャパシタの第１電極を形成する工程と、前記キャパシタの強誘電体膜を前記第１電極上に形成する工程と、前記キャパシタの第２電極を前記強誘電体膜上に形成する工程と、前記キャパシタの上方に膜を形成する工程とを有する半導体装置の製造方法において、前記キャパシタを形成した後の工程で、前記強誘電体膜中の還元作用を持つ粒子の濃度が1×10^{19}個／cm^3 未満となる条件で、前記トランジスタの特性を改善するために水素含有雰囲気中で前記半導体基板を加熱する工程を有することを特徴とする半導体装置の製造方法。

（６）前記粒子は、少なくとも水素原子と重水素原子のいずれかであることを特徴とする付記５に記載の半導体装置の製造方法。

（７）前記強誘電体膜は、スパッタ又はＭＯＣＶＤにより形成されることを特徴とする付記５又は付記６に記載の半導体装置の製造方法。

【００９５】

【発明の効果】以上述べたように本発明によれば、強誘電体膜の水素原子と重水素原子の濃度の総和を1×10^{19}個／cm^3 未満としたので、水素又は重水素に起因する強誘電体の劣化を防いで強誘電体キャパシタの特性を抑制できことが実験により明らかになった。また、水素原子と重水素原子の総和を1×10^{17}個／cm^3 未満とすることにより、その効果をさらに高めることができる。

【図面の簡単な説明】

【図１】図１は、本発明の実施形態に係る半導体装置の形成工程を示す断面図（その１）である。

【図２】図２は、本発明の実施形態に係る半導体装置の形成工程を示す断面図（その２）である。

【図３】図３は、本発明の実施形態に係る半導体装置の形成工程を示す断面図（その３）である。

【図４】図４は、本発明の実施形態に係る半導体装置の形成工程を示す断面図（その４）である。

【図５】図５は、本発明の実施形態に係る半導体装置の形成工程を示す断面図（その５）である。

【図６】図６は、本発明の実施形態に係る半導体装置の形成工程を示す断面図（その６）である。

【図７】図７は、本発明の実施形態に係る半導体装置の形成工程を示す断面図（その７）である。

【図８】図８は、本発明の実施形態に係る半導体装置の形成工程を示す断面図（その８）である。

【図９】図９は、本発明の実施形態に係る半導体装置の形成工程を示す断面図（その９）である。

【図１０】図１０は、本発明の実施形態に係る半導体装置の他の形成工程を示す断面図である。

【図１１】図１１は、本発明の実施形態に係る半導体装置を構成する強誘電体キャパシタの試料を示す断面図である。

【図１２】図１２は、本発明の実施形態に係る半導体装置のキャパシタを重水素処理した後のＳＩＭＳ分析による重水素濃度分布である。

【図１３】図１３は、本発明の実施形態に係る半導体装置のキャパシタ周辺領域を重水素処理した後のＳＩＭＳ分析による重水素濃度分布である。

【図１４】図１４は、本発明の実施形態に係る半導体装置のキャパシタ及びその周辺領域の強誘電体膜の重水素

処理時間と重水素濃度の関係を示す図である。

【図１５】図１５は、時間を変えて重水素処理された強誘電体キャパシタの電圧－分極特性を示す図である。

【図１６】図１６は、強誘電体キャパシタ初期の酸素、水素、重水素についてのＴＳＤ分析による濃度分布を示す図である。

【図１７】図１７は、強誘電体キャパシタのD_2加熱後の酸素、水素、重水素についてのＴＳＤ分析による濃度分布を示す図である。

【図１８】図１８は、IrO_2とＰＺＴを有するキャパシタのD_2による劣化のメカニズムである。

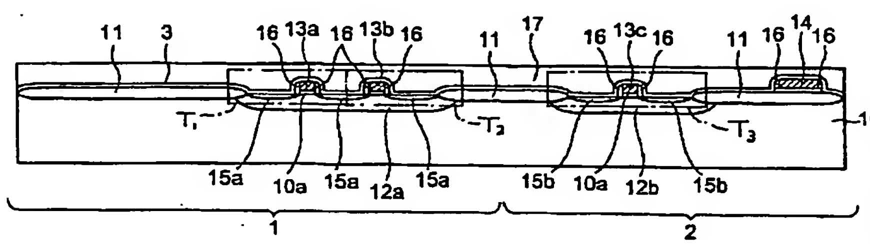
【図１９】図１９(a),(b) は、本発明に係る半導体装置のキャパシタの初期とD_2加熱後の強誘電体膜構成原子状態を示している。

【符号の説明】

１０…半導体基板、１１…素子分離絶縁膜、１２ａ，１２ｂ…ウェル領域、１３ａ，１３ｂ，１３ｃ…ゲート電極、１５ａ，１５ｂ…不純物拡散層、１６…サイドウォール、１７，２６，３１，３３、１８ａ～１８ｅ…プラグ、２１…SiON膜、２２…SiO_2膜、２３ａ，２５ａ…導電膜、２４ａ…強誘電体膜、２３…下部電極、２４…誘電体膜、２５…上部電極、２７…局所配線、３２ａ…局所配線、３２ｂ～３２ｇ…配線、３５…プラグ、３６…アルミニウム配線、３７，３８…カバー膜。

【図１】

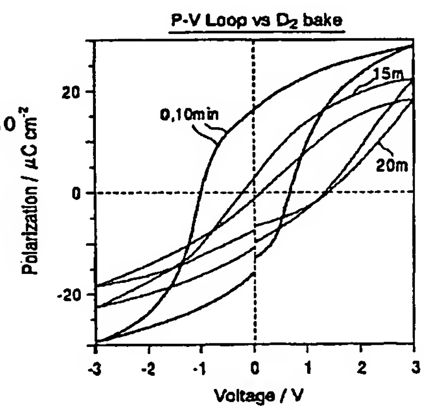
本発明の実施形態に係る半導体装置の形成工程を示す断面図（その１）



10：半導体基板
12a,12b：ウエル領域
17：層間絶縁膜
11：素子分離絶縁膜
10a：ゲート絶縁膜
13a～13c：ゲート電極
14：配線
15a：n型不純物拡散領域
15b：p型不純物拡散領域
16：側壁絶縁膜
3：カバー膜
Ｔ１～Ｔ３：ＭＯＳトランジスタ

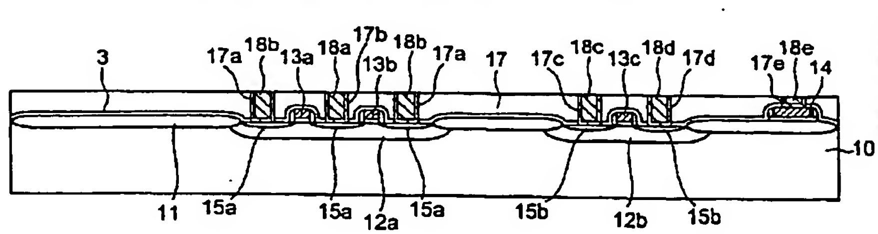
【図１５】

時間を変えて重水素処理された強誘電体キャパシタの電圧－分極特性



【図２】

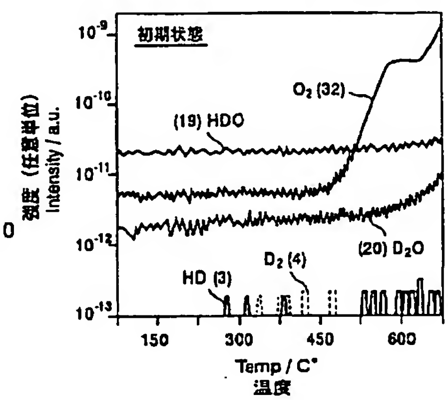
本発明の実施形態に係る半導体装置の形成工程を示す断面図（その２）



１７ａ～１７ｄ：コンタクトホール
１７ｅ：ビアホール
１８ａ～１８ｃ：プラグ

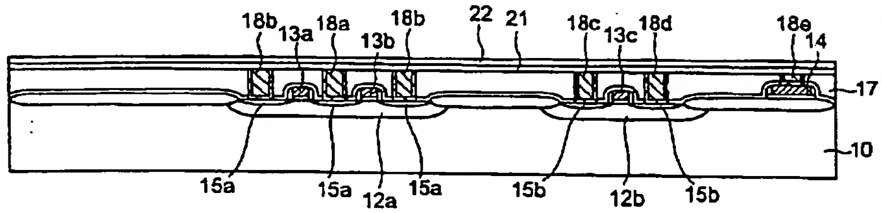
【図１６】

強誘電体キャパシタ初期の酸素、水素、重水素についてのTSD分析による濃度分布



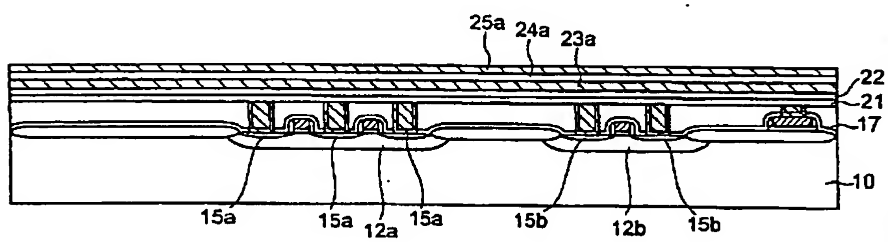
【図３】

本発明の実施形態に係る半導体装置の形成工程を示す断面図（その３）



【図４】

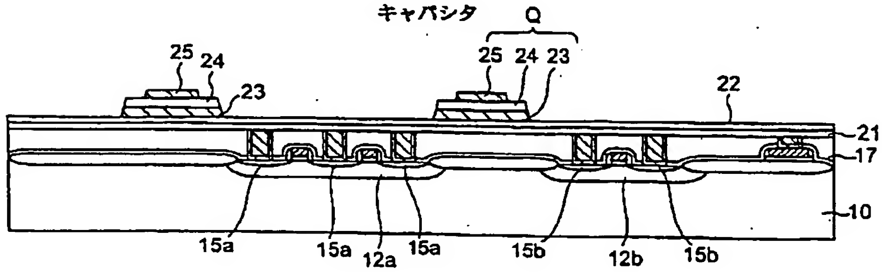
本発明の実施形態に係る半導体装置の形成工程を示す断面図（その４）



２３ａ：第１導電体膜
２４ａ：強誘電体膜
２５ａ：第２導電体膜

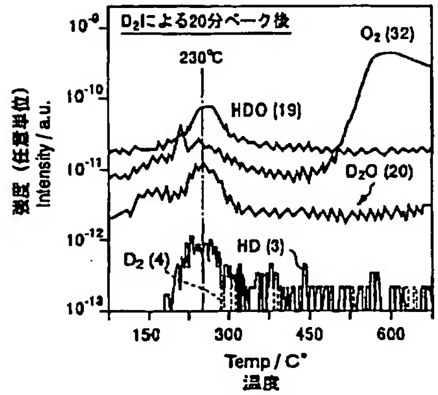
【図５】

本発明の実施形態に係る半導体装置の形成工程を示す断面図（その５）



【図１７】

強誘電体キャパシタのD₂加熱後の酸素、水素、重水素についてのTSD分析による濃度分布



【図１８】

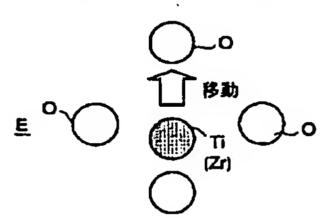
IrO₂とPZTを有するキャパシタのD₂による劣化のメカニズム

1. $IrO_2 \rightarrow Ir + O_2$ (真空還元、副次的)
2. $IrO_2 + D_2 \rightarrow Ir + D_2O$ (化学還元)
3. $Ir + D_2 \rightarrow 2D^+(Ir)$ (上部電極触媒反応：主的)
4. $Pt + D_2 \rightarrow 2D^+(Ir)$ (下部電極触媒反応：主的)
5. $D^+ + PZT \rightarrow PZT\text{-}D$ (境界拡散及びQsw低減)

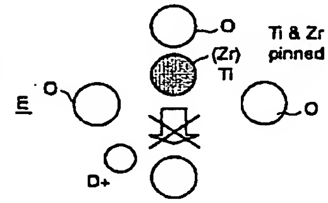
【図１９】

本発明に係る半導体装置のキャパシタの初期とD₂加熱後の強誘電体構成電子状態

(a)　初期のPZTのペロヴスカイト構造

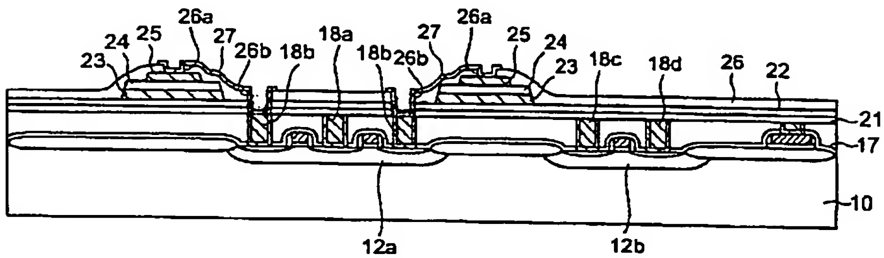


(b)



【図６】

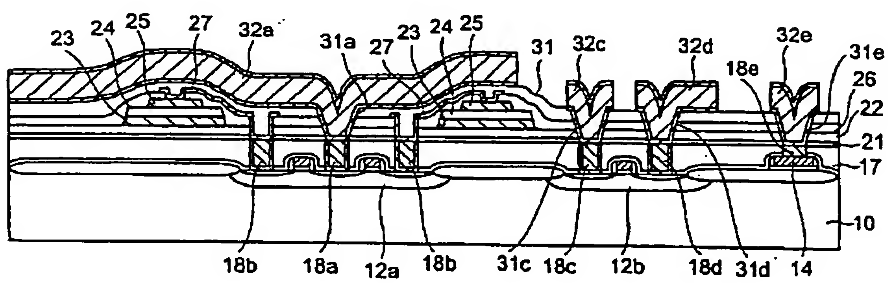
本発明の実施形態に係る半導体装置の形成工程を示す断面図（その６）



２６：層間絶縁膜
２７：局所配線

【図７】

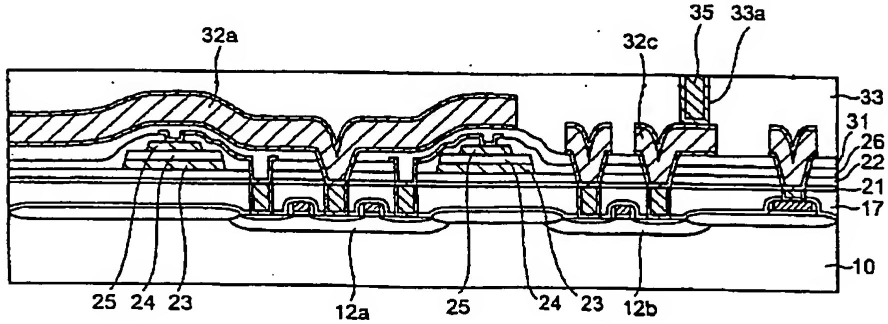
本発明の実施形態に係る半導体装置の形成工程を示す断面図（その７）



３２ａ：ビット線
３２ｂ～３２ｅ：配線

【図８】

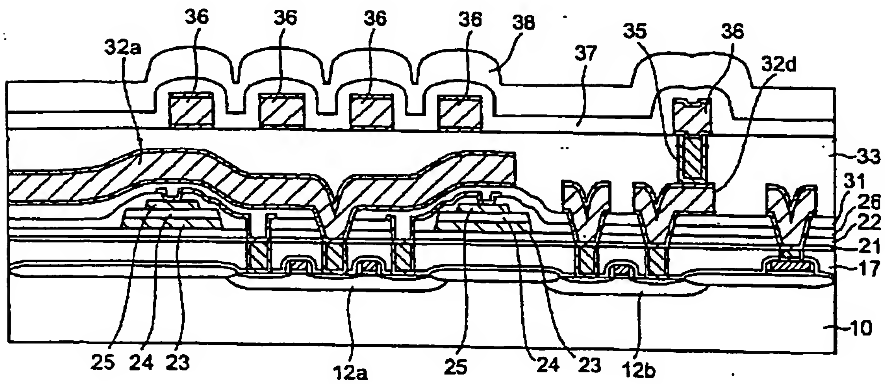
本発明の実施形態に係る半導体装置の形成工程を示す断面図（その８）



３３：層間絶縁膜

【図９】

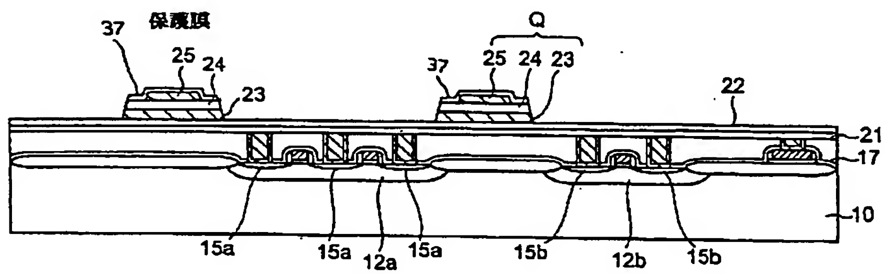
本発明の実施形態に係る半導体装置の形成工程を示す断面図（その９）



３６：配線
３７，３８：カバー膜

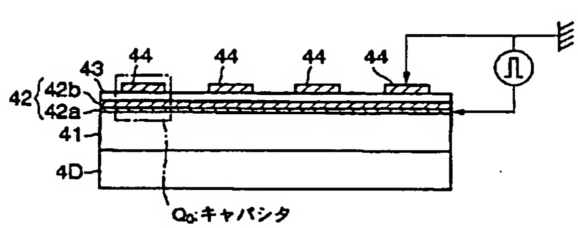
【図１０】

本発明の実施形態に係る半導体装置の他の形成工程を示す断面図



【図１１】

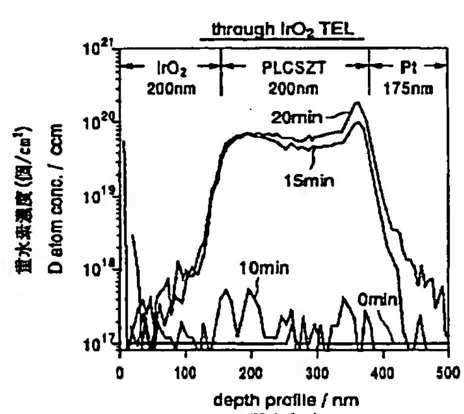
本発明の実施形態に係る半導体装置を構成する強誘電体キャパシタ



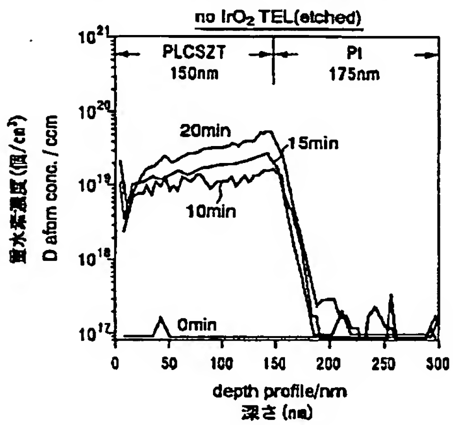
42:下部電極
43:強誘電体膜
44:上部電極

【図１２】

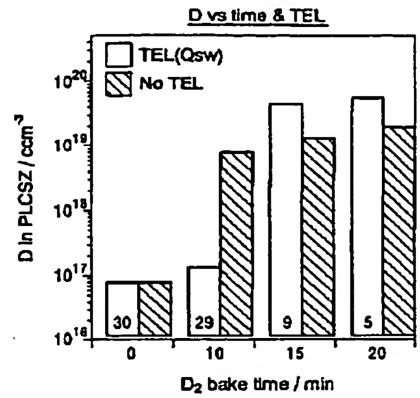
本発明の実施形態に係る半導体装置のキャパシタを重水素処理した後のSIMS分析による重水素濃度分布



【図１３】



【図１４】



フロントページの続き

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Ｆターム(参考)　5F083 FR02 GA21 JA15 JA17 JA36
JA38 JA39 JA40 JA43 MA06
MA17 MA19 MA20 NA01 NA08
PR33 PR34 PR39 PR40 PR41

(translation of OA)

Mailing Date: April 21, 2004

NOTICE OF REASON FOR REJECTION

Japanese Patent Application No. 2003-153693

Preparation Date: April 16, 2004

From Masayuki OGAWA, Examiner of the Patent Office

To Agent: Motohiko FUJIMURA

Applied Article: Article 29, para. 1, and Article 29, para. 2

It is considered that the above-identified patent application should be rejected for the reason set forth hereunder. In case the applicant wishes to raise an argument against this decision, the applicant is required to submit the argument within 60 days from the mailing date of this notice.

Reason for Rejection

1. It is considered that the inventions as set forth in the following claims of this application are the same inventions which are described in the following publications which have been distributed in Japan or abroad, or are made available to the public through electric telecommunication lines, prior to the filing date of this application. Therefore, this application cannot be patented under the provision of Article 29, para. 1 subpara. 3 of the patent law.

2. It is considered that the inventions as set forth in the following claims of this

application are deemed to have easily been conceived prior to the filing date of this application by those who have ordinary knowledge in the technical field it belongs to, on the basis of the inventions described in the following publications which have been distributed in Japan or abroad or made available to the public through electric telecommunication lines, prior to the filing date of this application. Therefore, this application cannot be patented under the provision of Article 29, para. 2 of the patent law.

Notes (See the list of cited references etc., below.)

・ Regarding the invention in claims 1-2, 5-7

Reasons 1, 2

Cited reference 1

<Remark>

See especially paragraphs 【0099】 - 【0120】 and Figs. 14 – 18 of the cited reference 1.

・ Regarding the invention in claims 3-4, 8

Reasons 2

Cited reference 1-3

<Remark>

To mount a ferroelectric capacitor on a plug oxidation protective film is a publicly known art disclosed in the cited reference 2. (See paragraphs 【0021】- 【0067】and Figs. 1 –9 .) Furthermore, to form a hydrogen diffusion preventing layer on side surfaces of a ferroelectric capacitor is a publicly known art disclosed in the cited reference 3.

For the claim other than the claims specified in this notice of reason for rejection i.e. claim 9, no reason for rejection is found at present. If any reason for rejection is found later, it will be notified.

The list of cited references etc.

1 Japanese Patent Kokai No. 11-17124

2 Japanese Patent Kokai No. 2003-86776

3 Japanese Patent Kokai No. 2002-353414

Record of the result of prior art search

- Technical fields to be searched Int. Cl(7)

  H01L 21/8229

  H01L 21/8239 – 21/8247

  H01L 27/10 – 27/115

- Prior Arts But Not Applied

No prior art references are found other than the references cited in the present notice of reason for rejection.

This record is not a component of the reason for rejection.

In case the applicant wishes to ask any questions concerning this notice of reason for rejection or to have an interview with the examiner regarding this application, please contact:

Masayuki OGAWA

Semiconductor division, third patent examination department

(Tel) 03-3581-1101 Extn. 3462

(fax)03-3501-0673

拒絶理由通知書

特許出願の番号	特願２００３－１５３６９３
起案日	平成１６年　４月１６日
特許庁審査官	小川　将之　　　　　９６３４　４Ｍ００
特許出願人代理人	藤村　元彦　様
適用条文	第２９条第１項、第２９条第２項

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この出願は、次の理由によって拒絶をすべきものである。これについて意見があれば、この通知書の発送の日から６０日以内に意見書を提出して下さい。

理　由

１．この出願の下記の請求項に係る発明は、その出願前に日本国内又は外国において、頒布された下記の刊行物に記載された発明又は電気通信回線を通じて公衆に利用可能となった発明であるから、特許法第２９条第１項第３号に該当し、特許を受けることができない。

２．この出願の下記の請求項に係る発明は、その出願前日本国内又は外国において頒布された下記の刊行物に記載された発明又は電気通信回線を通じて公衆に利用可能となった発明に基いて、その出願前にその発明の属する技術の分野における通常の知識を有する者が容易に発明をすることができたものであるから、特許法第２９条第２項の規定により特許を受けることができない。

記　　（引用文献等については引用文献等一覧参照）

・請求項１－２，５－７
　理由１，２
　引用例１
＜備　考＞
　引用例１の【００９９】～【０１２０】段落及び第１４図～第１８図を特に参照。

・請求項３－４，８
　理由２
　引用例１－３
＜備　考＞
　プラグ酸化防止膜上強誘電体キャパシタを形成する点は引用例２（【００２１

】～【００６７】段落及び第１図～第９図を参照。）に記載されている公知技術である。また、水素拡散防止膜を強誘電体キャパシタ側面に形成する技術は引用例３に記載されている公知技術である。

この拒絶理由通知書中で指摘した請求項以外の請求項９に係る発明については、現時点では、拒絶の理由を発見しない。拒絶の理由が新たに発見された場合には拒絶の理由が通知される。

引　用　文　献　等　一　覧

1.特開平１１－１７１２４号公報
2.特開２００３－８６７７６号公報
3.特開２００２－３５３４１４号公報

－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－

先行技術文献調査結果の記録

・調査した分野　ＩＰＣ第７版
　Ｈ０１Ｌ　２１／８２２９
　Ｈ０１Ｌ　２１／８２３９－２１／８２４７
　Ｈ０１Ｌ　２７／１０－２７／１１５

・先行技術文献
　拒絶理由通知で引用したもの以外に無し。

この先行技術文献調査結果の記録は、拒絶理由を構成するものではない。

－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－－

この拒絶理由通知の内容に関するお問い合わせ、または面接のご希望がございましたら下記までご連絡下さい。

特許審査第三部半導体機器　小川　将之（おがわ　まさゆき）
ＴＥＬ．０３（３５８１）１１０１　内線３４６２
ＦＡＸ．０３（３５０１）０６７３